CHAPTER 2

PC System Boards

Terms you'll need to understand:

- ✓ Slot 1
- ✓ Slot 2
- ✓ Slot A
- ✓ Socket A
- ✓ Socket 7
- ✓ Socket 8
- ✓ Socket 423
- ✓ Socket 478
- ✓ Socket 370
- ✓ Socket LGA775
- ✓ Socket 939
- ✓ PCI slots
- ✓ PCI-X slots
- ✓ PCIe sLots
- ✓ AGP slots
- ✓ Chipsets
- ✓ USB (Universal Serial Bus) interface
- ✓ FireWire interface
- ✓ AMR (audio modem riser) slots
- ✓ CNR (communication network riser) slots
- ✓ PATA interfaces
- ✓ SATA interfaces
- ✓ SCSI interfaces
- ✓ CMOS setup

Techniques to master:

- ✓ Essentials 1.1—Identify the fundamental principles of using personal computers.
- ✓ Identify the names, purposes, and characteristics of motherboards.
- ✓ Form factor (for example, ATX / BTX, micro ATX / NLX)
- ✓ Components
  - ✓ Integrated I/Os (for example, sound, video, USB, serial, IEEE 1394 / FireWire, parallel, NIC, modem)
  - ✓ Memory slots (for example, RIMM, DIMM)
  - ✓ Processor sockets
  - ✓ External cache memory
  - ✓ Bus architecture
  - ✓ Bus slots (for example, PCI, AGP, PCIE, AMR, CNR)
  - ✓ EIDE/PATA
  - ✓ SATA
  - ✓ SCSI technology
  - ✓ Chipsets
  - ✓ BIOS/CMOS/Firmware
  - ✓ Riser card/daughter board

Introduction

This chapter covers the motherboard areas of the CompTIA A+ Certification—Essentials examination under Objective 1.1. The system board is the main component in a PC-compatible microcomputer system. The system board contains the components that form the basis of the computer system. Even though the system board's physical structure has changed over time, its logical structure has remained relatively constant. Since the original PC, the system board has contained the microprocessor, its support devices, the system's primary memory units, and the expansion-slot connectors.

Technicians must be aware of the characteristics of different types of system boards in the marketplace. This will enable them to make intelligent choices about repairing, upgrading, or exchanging system boards.

System Board Form Factors

Although the term *form factor* generally refers to the physical size and shape of a device, with system boards it also refers to their case style and power supply compatibility, as well as to their I/O connection placement schemes. These factors must be considered when assembling a new system from components, and in repair and upgrade situations where the system board must be replaced.

One of the first considerations when installing or replacing a system board is whether it will physically fit (form factor) and work with the other system components (compatibility). In both of these situations, the following basic issues must be dealt with: the system board's form factor, its case style, and its power-supply connection type.

NOTE

CompTIA's 2006 A+ exam deals only with ATX, BTX, and NLX form factors.

ATX System Boards

Intel developed the ATX form factor for Pentium-based systems as an evolution of the older Baby AT form factor that first integrated the standard I/O functions onto the system board. It has been the predominant PC form factor for some time. The ATX specification basically rotates the Baby AT form factor by 90 degrees, relocates the power-supply connection, and moves the microprocessor and memory modules away from the expansion slots.

Figure 2.1 depicts a Pentium-based ATX system board that directly supports the floppy disk drive (FDD), hard disk drive (HDD), serial, and parallel ports. The board is 12 inches (305mm) wide and 9.6 inches (244mm) long. A revised mini-ATX specification allows for 11.2 inch-by-8.2 inch system boards. The mounting-hole patterns for the ATX and mini-ATX system boards require a case that can accommodate ATX boards.

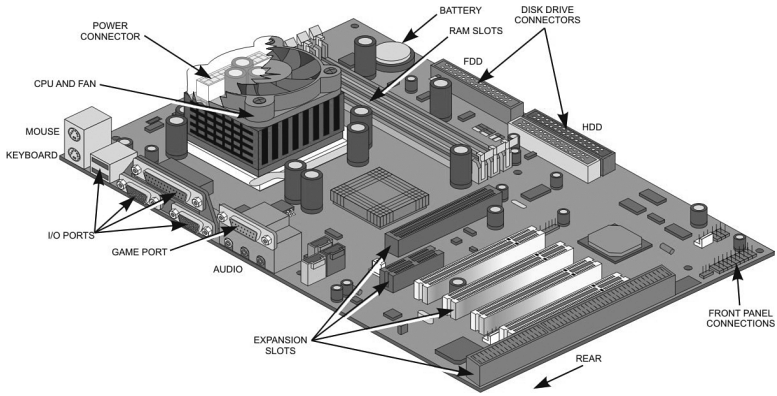


FIGURE 2.1 An ATX Pentium system board.

EXAM ALERT

Be able to identify the major components of an ATX system board from a graphical representation.

The power-supply orientation enables a single fan to be used to cool the system. This feature results in reduced cost, reduced system noise, and improved reliability. The relocated microprocessor and memory modules enable full-length adapter cards to be used in the expansion slots while providing easy upgrading of the microprocessor, RAM, and I/O devices.

The fully implemented ATX format also has specifications for the power-supply and I/O connector placements. In particular, the ATX specification for the power-supply connection calls for a single 20-pin power cord between the system board and the power-supply unit. This cable provides a +3.3V (DC) supply along with the traditional +/– 12V (DC) and +/– 5V (DC) supplies. A software-activated power switch can also be implemented through the ATX power-connector specification. The PS-ON and 5VSB (5V Standby) signals can be controlled by the operating system to perform automatic system shutdowns.

As mentioned in Chapter 1, "Basic PC Terms and Concepts," newer ATX power supplies include a 4-pin, 12V EPS clip-on extension to the standard 20-pin ATX power connector. The additional conductors provide additional current-carrying capabilities to support newer microprocessors and high-end peripherals.

BTX System Boards

The BTX form factor specification is designed to provide better thermal handling capabilities, better acoustic characteristics, and provisions for newer PC technologies. The BTX form factor is not compatible with the older ATX specification. It moves key components, such as the microprocessor, chipset, and video controller, to new general locations on the system board to achieve better airflow (and cooling) characteristics inside the system unit. Figure 2.2 depicts the recommended full-size version of a BTX system board.

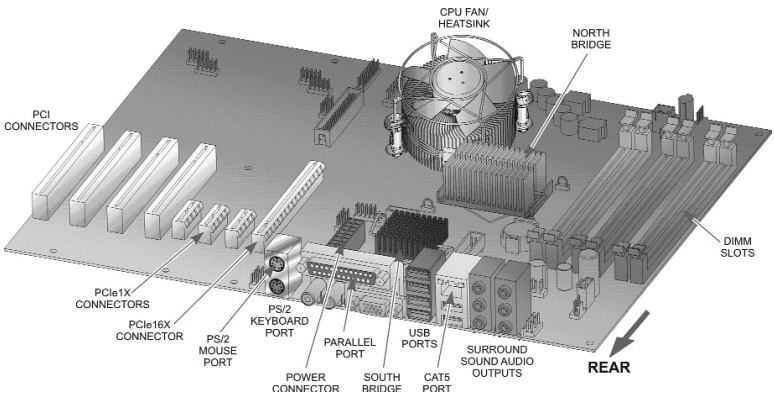


FIGURE 2.2 BTX system board.

The microprocessor has been moved toward the front center section of the board, as have the chipset devices. The major source of cooling in the BTX system is the *thermal module* depicted in Figure 2.3. The thermal module mounts to the front of the system unit and sits directly over the microprocessor and chipset components to provide inline airflow across the components. This reduces the need for additional cooling fans and heat sinks, which in turn lowers the cost of the unit. BTX thermal modules come in two varieties: a standard height Type I version, which is designed for full-height cases, and a low-profile Type II version designed for small form factor cases.

This configuration also improves the *acoustics* of the unit, which is becoming an area of greater concern as PCs are increasingly being used as media servers. *Media servers* are specialized PCs designed specifically for delivering audio and

video services in the home setting. In these applications, the sound levels generated by cooling and case fans can reach unacceptable levels.

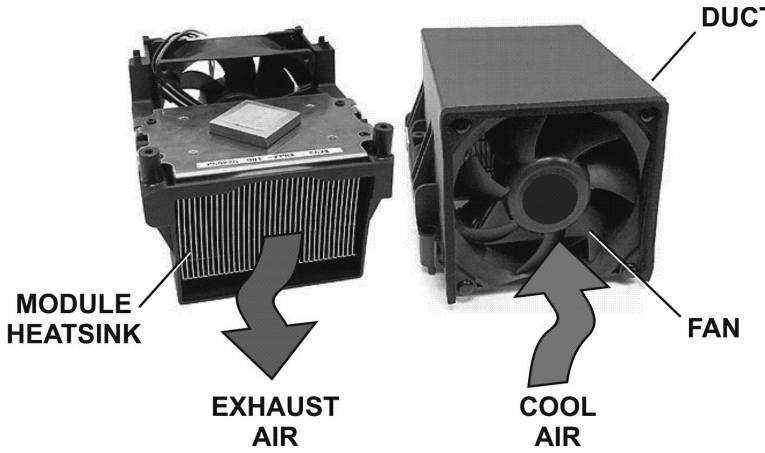


FIGURE 2.3 BTX thermal modules draw cool air in from the top, pulling it over the top of the processor and venting the heated air from the vents on the sides of the module.

BTX Options

The BTX specification offers four board widths that share common core design characteristics. The length of all the board types is 266.7mm. One of the core design characteristics is that in each version the expansion slots have been moved to the right side of the BTX boards, making BTX designs incompatible with other PC form factors. The standard BTX board versions are described in Figure 2.4 and include the following:

- PicoBTX—This is the smallest BTX variation at a width of 203.2mm. It includes only a single expansion slot.
- NanoBTX—This BTX version increases the board width to 223.53mm and provides for two expansion slots.
- Micro BTX—This medium-size BTX version includes four expansion slots on a board that is increased to a width of 264.16mm.
- BTX—The full-size BTX specification extends the number of expansion slots from the four in the smaller variations to a total of seven. The board width for the full version is 325.12mm.

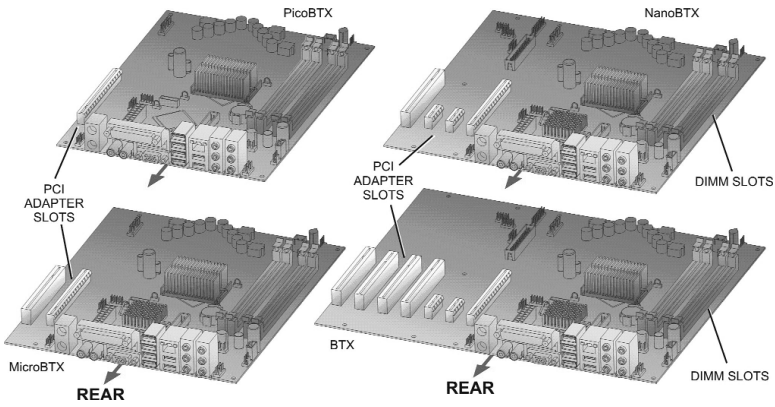


FIGURE 2.4 Standard BTX size variations.

BTX system boards routinely include SATA interface connections, USB 2.0 ports, and PCI Express (PCIe) expansion slots. The larger the board, the more adapter slots and slot types are included. Typical expansion slots used in BTX systems include PCI-5V, PCI-3.3V, AGP-3.3V, AGP-1.5V, and PCI Express slots. The dual inline memory module (DIMM) slots are located near the microprocessor and its chipset components.

The various BTX system board sizes are intended to allow the same technologies to be used in tower, desktop, and low-profile configurations. Figure 2.5 illustrates how these variations are implemented in the different case styles.

The BTX specification makes provisions for using ATX power supplies as well as low-profile form factor (LFX) and compact form factor (CFX) small form factor power supplies.

The BTX back panel moves the rear panel I/O connectors, depicted in Figure 2.6, to the center of the back panel. This layout is the result of better placement of the I/O controller on the system board. Most BTX back panels include PS/2 mouse and keyboard connectors, VGA (Video Graphics Array) video connections, and legacy parallel printer/serial ports. In addition, the BTX back panel may offer a variety of consumer audio and video connection combinations.

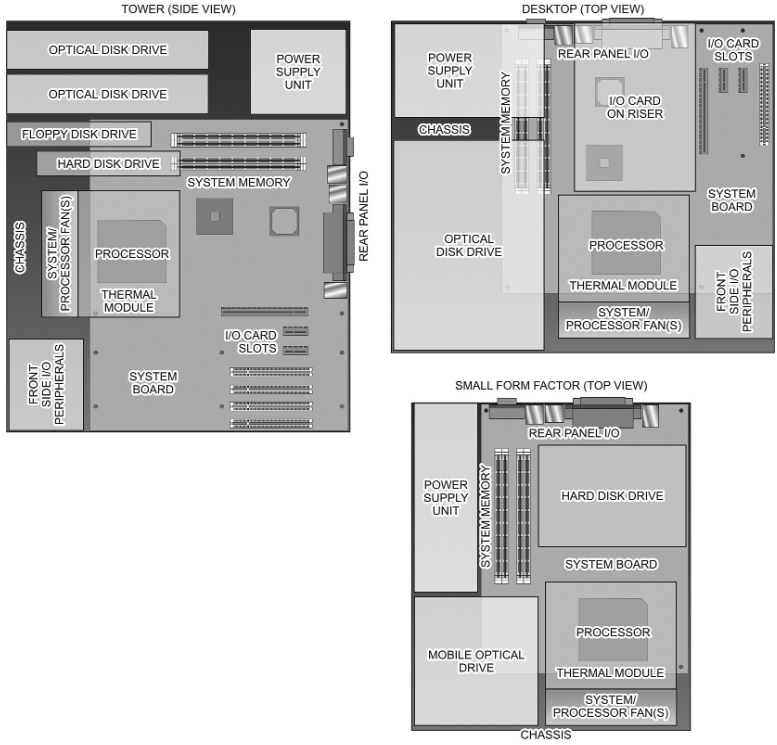


FIGURE 2.5 BTX implementations.

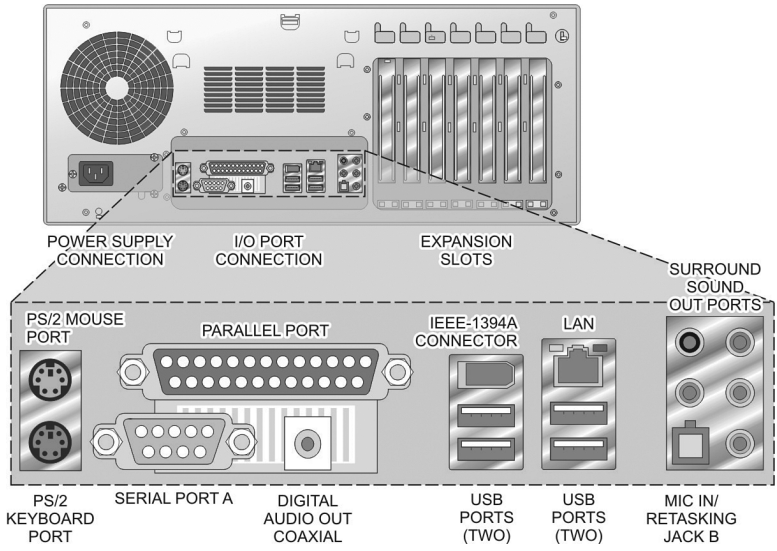


FIGURE 2.6 Typical BTX back panel layout.

Low-Profile Form Factors

Low-profile cases employ short backplanes to provide a lower profile than traditional desktop units. In low-profile cases, the adapter cards are mounted horizontally on the backplane card that extends from an expansion slot on the motherboard. The expansion slot openings in the back panel of the case are horizontal as well. To accommodate the lower profiles, special lowered power supply versions have also been developed.

The low-profile extended (LPX) form factor, also referred to as the slim-line form factor, was designed to reduce the height of the system unit. As such, the specification applied to system unit cases, power supply units, and expansion cards. LPX never became an official standard but it gained enough industry support that millions of cases and power supply units were produced. LPX system boards typically incorporated built-in video so that no adapter card was needed for this function. Finally, LPX units typically had poor ventilation characteristics—the low case height and horizontally mounted adapter cards tended to trap heat near the system board surface.

The new low-profile extended (NLX) form factor, depicted in Figure 2.7, did become a legitimate standard for cases, power supplies, and system boards. However, manufacturers have chosen to produce low-profile units based on microATX and miniATX designs. These form factors followed the ATX design specification but reduced the size of the unit (and its associated costs) by limiting the number of expansion slots.

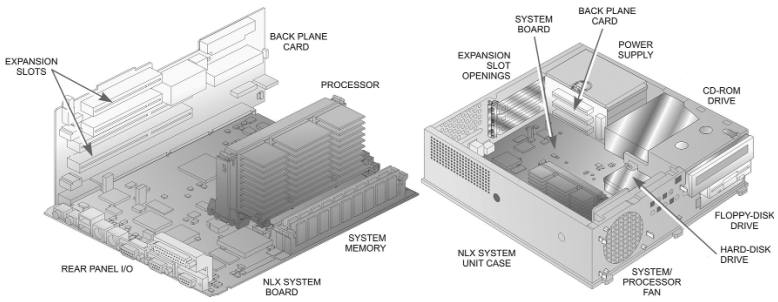


FIGURE 2.7 NLX components.

Pentium Chipsets

Integrated circuit manufacturers develop different chipsets to support different processor types. The typical Pentium chipset consists of a memory controller (called the *North Bridge*), a PCI host bridge (referred to as the *South Bridge*), and

in some older versions, a Super (or enhanced) I/O controller. The memory controller provides the interface between the system's microprocessor, its various memory sections, and the PCI bus.

In turn, the host bridge monitors the microprocessor's address bus to determine whether addresses are intended for devices on the system board, in a Peripheral Component Internconnect (PCI) slot, or in one of the system board's other expansion slots. It also provides the interface between the PCI bus, the IDE (Integrated Drive Electronics) bus, and the ISA bus (if present). The Super I/O controller chip interfaces the standard PC peripherals (LPT, COM, and FDD interfaces) to the ISA bus.

This typical chipset arrangement may vary for a couple of reasons. The first is to include a specialized function, such as an advanced graphics port (AGP) or USB interface. The second reason is to accommodate changes in bus specifications such as PCI-X or PCIe slots. Figure 2.8 shows an advanced Pentium/PCI chipset design that includes an AGP slot. Notice that the AGP slot is local to the North Bridge—meaning that it has very fast access to the microprocessor.

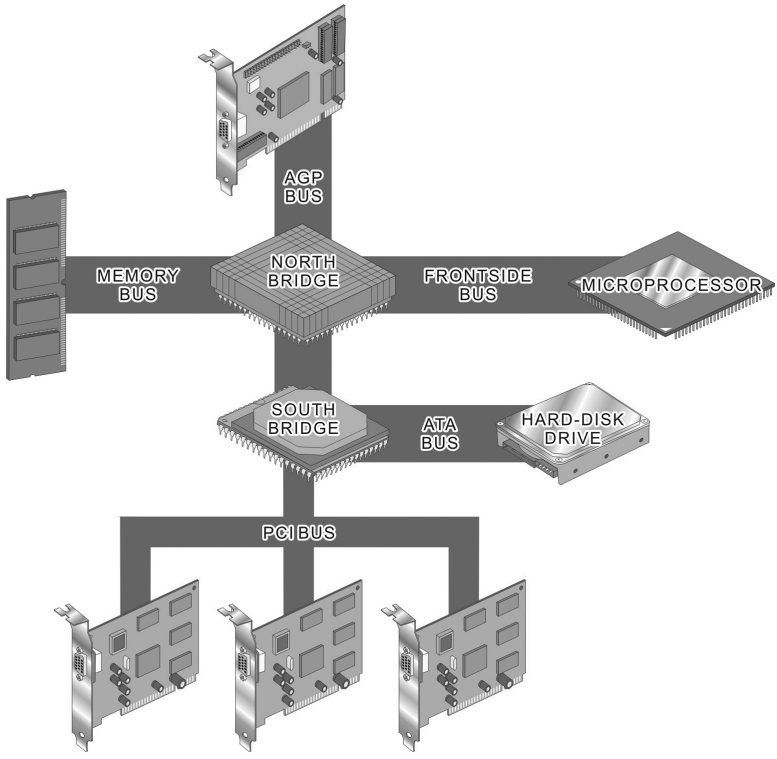


FIGURE 2.8 Pentium chipset with an AGP slot.

Figure 2.9 depicts an advanced Pentium/PCI chipset that provides advanced PCIe expansion buses for multiple "links." Notice that each PCIe link is attached directly to the South Bridge (with the exception of a special PCIe link for the high-end video display adapter).

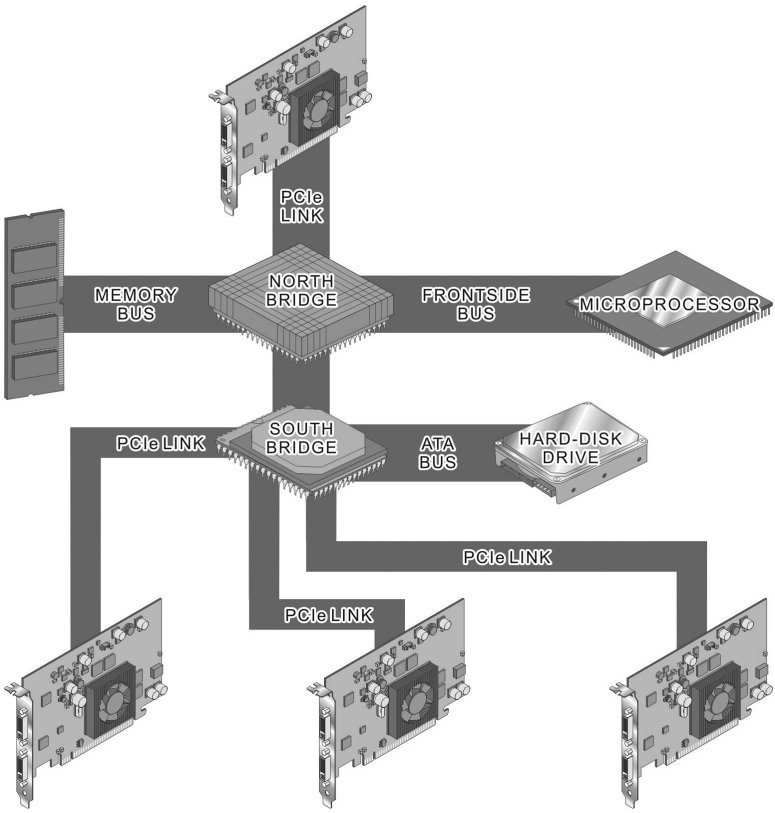


FIGURE 2.9 Advanced Pentium/PCIe chipset.

It is normal to consider the ROM BIOS as an integral part of any chipset model because it is designed to support the register structure of a particular chipset. One of the major functions provided by the BIOS is the Chipset Features configuration screen in the CMOS setup routine described later in this chapter.

Technicians can use this tool to optimize the system settings to provide maximum internal performance. However, these settings tend to be very technical and require an extensive understanding of the specific system's component structure to configure. Therefore, replacing a ROM BIOS chip on a system board is not as simple as placing another ROM BIOS IC (integrated circuit) in

the socket. The replacement BIOS must have correct information for the specific chipset it is being used with.

Dual-Core Intel Chipsets

Intel has also introduced a new series of system board chipsets to support the Pentium D line of processors. These include the Intel 975X, 955X, 945G, 945GZ, 945P, and 945PL Express chipsets. Figure 2.10 depicts the block diagram of a typical Pentium D processor chipset. The chipset described in the figure is the 955X chipset. This chipset is primarily intended to support Pentium D and Pentium Extreme Edition processors. However, Intel also lists it as supporting all other Intel microprocessors using the LGA775 socket.

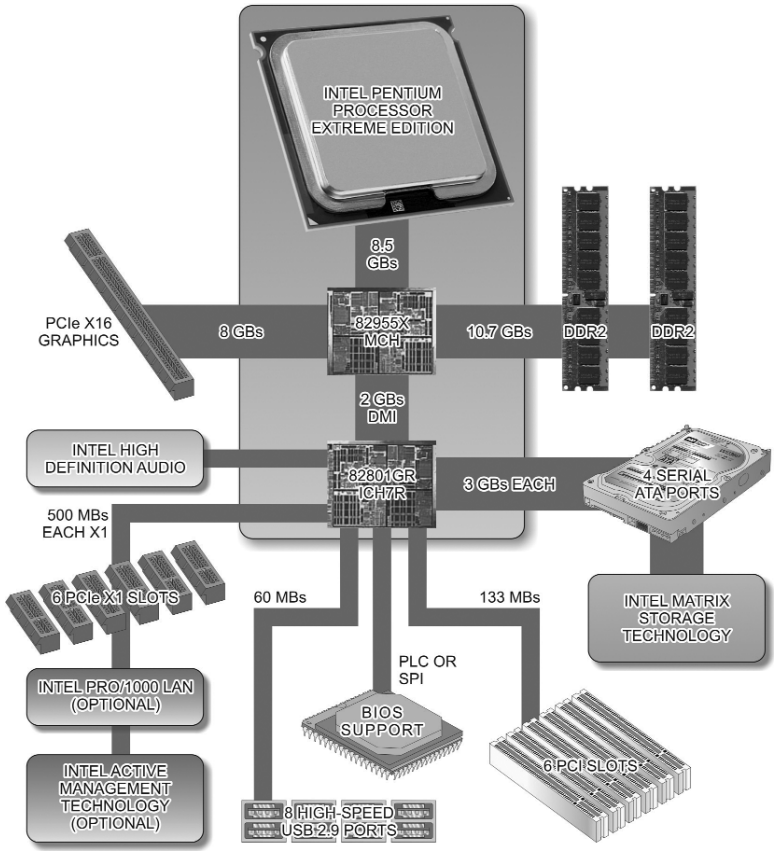


FIGURE 2.10 An Intel dual-core processor chipset.

Chipsets designed to support the Pentium Extreme Edition processors with hyperthreading technology include the Intel 975X, 955X, 945G, 925XE, 925X,

and 915G Express chipsets. Figure 2.11 depicts the block diagram of a typical Pentium Extreme Edition processor chipset. This particular chipset is the 975X chipset designed for high-performance gaming, multimedia, and business applications. Notice the extremely fast front side bus capabilities, the number of PCIe options available, and the number of different I/O options supported.

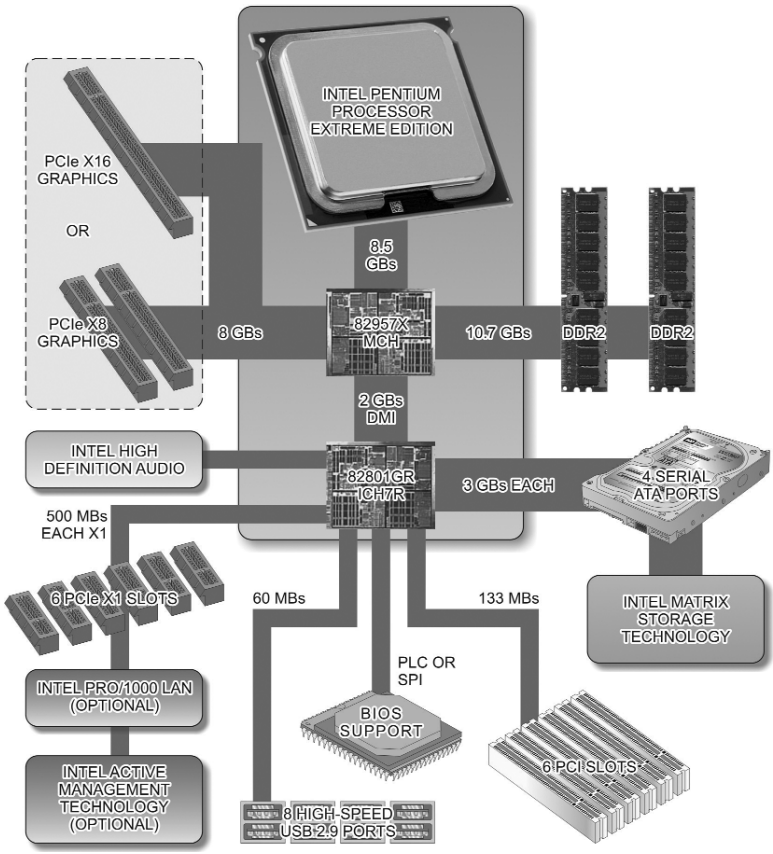


FIGURE 2.11 An Intel Pentium Extreme Edition chipset.

The 910GL Express chipset is used with the Intel Celeron D processor. Likewise, a low-power chipset has been developed to support the Core Duo processors in mobile computing environments. This chipset is the Intel 945GTExpress chipset. Figure 2.12 depicts the block diagram of the Pentium Celeron D processor chipset. Notice the reduced set of features compared to the previous chipset architectures. Also notice the reduced speeds associated with the major buses and I/O connections.

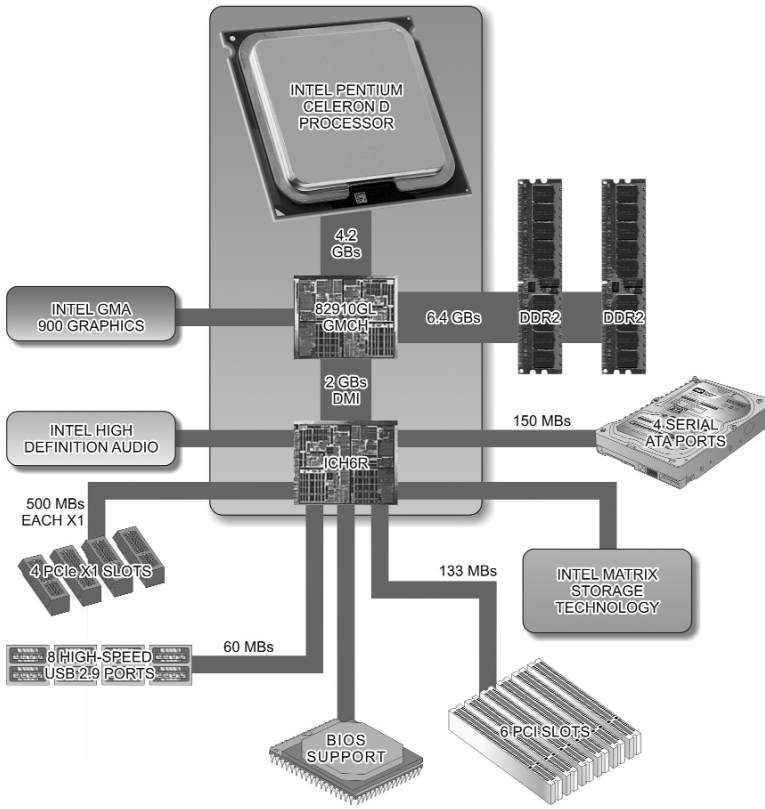


FIGURE 2.12 An Intel Pentium Celeron D chipset.

Table 2.1 compares the attributes of the different dual-core Pentium chipsets.

TABLE 2.1 Dual-Core Pentium Chipset Specifications

PRODUCT	FSB SPEEDS	MEMORY TYPES	EXPANSION BUSES	DISK DRIVE SUPPORT
Pentium D				
975X Express	800/1066	DDR2.533 /667 (8GB)	PCIe × 16/×1	SATA – 3Gbps
945G Express	533/800/ 1066	DDR2.400/ 533/667	PCIe × 16/×1 (4/6)	SATA – 3Gbps/4
945GZ Express	533/800	DDR2.400/ 533	PCIe × 1 (4/6)	SATA – 3Gbps/4

TABLE 2.1 *Continued*

PRODUCT	FSB SPEEDS	MEMORY TYPES	EXPANSION BUSES	DISK DRIVE SUPPORT
945P Express	533/800/1066	DDR2.400/533/667	PCIe ×16/×1 (4/6)	SATA – 3Gbps/4
945PL Express	533/800	DDR2.400/533	PCIe ×16/×1 (4/6)	SATA – 3Gbps/4
Pentium EE				
975X Express	800/1066	DDR2.533/667 (8GB)	PCIe ×16/×1	SATA – 3Gbps
955X Express	800/1066	DDR2.533/667 (8GB)	PCIe ×16/×1	SATA – 3Gbps
945G Express	533/800/1066	533/800/1066	PCIe ×16/×1 (4/6)	SATA – 3Gbps
925XE Express	800/1066	DDR2.400/533	PCIe ×16/×1	SATA – 1.5Gbps
925X Express	800	DDR2.400/533	PCIe ×16/×1	SATA – 1.5Gbps
915G Express	533/800	DDR/DDR2.533	PCIe ×16/×1	SATA – 150Mbps
Celeron D				
910GL Express	533	DDR-333/400	PCIe ×1 (4/6)	SATA – 150Mbps

System Bus Speeds

Microprocessor and chipset manufacturers are continually developing products to speed up the operation of the system. The first method used to speed up the system is to separate the speed at which the internal core of the processor runs from that of all the buses and devices external to it. In the Pentium processor, two speed settings can be established for the microprocessor—one is the *core speed* at which the internal microprocessor operations take place, and the second is a derivative bus speed for its external bus transfers. These two operational speeds are tied together through an internal clock multiplier system.

The second method is to speed up the movement of data across its data buses. As the previous chipset figures in this chapter have shown, the buses operating directly with the microprocessor and North Bridge, referred to as the *Front Side Bus (FSB)*, are running at one speed, whereas the PCI bus is running at a

different speed, and the peripheral devices are running at still another speed. In Pentium processors, a parallel bus called the *Back Side Bus (BSB)* connects the microprocessor with its internal L2 cache.

The chipset devices are responsible for coordinating data and control signal flow between the different buses (much like highways and streets where traffic travels at different speeds). The devices in the chipset act as on/off ramps and stoplights to effectively coordinate information movement across the buses. For example, with a current Pentium system board, the processor may run at 3.0GHz internally, while the front side bus runs at 800MHz (200 MHz × 4), the PCI bus runs at 33MHz, and the IDE bus runs at 100MHz.

Expansion Slots

The system's expansion slots provide the connecting point for most of its I/O devices. Interface cards communicate with the system through the extended microprocessor buses made available through these slots. The PCI expansion bus specification has become the dominant expansion bus and slot configuration for PCs. Continued advancement of the PCI architecture has prevented it from being replaced by another type of bus/slot architecture.

The original ATX Pentium class system boards contained a mixture of ISA and PCI slots. Subsequent generations added AMR or CDR slots for specialized audio/modem functions. Most of these designs also added an AGP slot to support high-speed video display functions. Current ATX and BTX designs have completely discarded the ISA, AGP, AMR/CDR slots, and provide different versions of the PCI slot (that is, PCI and PCI-X or PCI and different PCIe slot types).

With the exception of the ISA slot, all the other expansion bus specifications mentioned include slot-addressing capabilities and reserve memory space to allow for plug-and-play reconfiguration of each device installed in the system. However, because no identification or reconfiguration capabilities were designed into the ISA bus specification, the presence of ISA-compatible slots on the system board can seriously disrupt plug-and-play operations.

PCI Local Bus

The Peripheral Component Interconnect local bus design incorporates three elements: a low-cost, high-performance local bus; the automatic configuration of installed expansion cards (PnP); and the capability to expand with the introduction of new microprocessors and peripherals. The data-transfer performance

of the PCI local bus is 132MBps using a 32-bit bus and 264MBps using a 64-bit bus. This is accomplished even though the bus has a maximum clock frequency of 33MHz.

The PCI peripheral device has 256 bytes of onboard memory to hold information as to what type of device it is. The peripheral device can be classified as a controller for a mass-storage device, a network interface, a display, or other hardware. The configuration space also contains control, status, and latency timer values. The latency timer register on the device determines the length of time that the device can control the bus for bus-mastering operations.

The PCI bus specification uses multiplexed address and data lines to conserve the pins of the basic 124-pin PCI connector. Within this connector are signals for control, interrupt, cache support, error reporting, and arbitration.

The original PCI bus employed 32-bit address and data buses. Its specification also defined a 64-bit multiplexed address and data bus variation for use with 64-bit processors, such as the Pentium. Its clock line was originally defined for a maximum frequency of 33MHz and a 132MBps transfer rate; however, it can be used with microprocessors operating at higher clock frequencies (66MHz under the PCI 2.1 specification).

The PCI 2.2 and PCI 2.3 versions of the bus implemented two new slot structures to provide a true 64-bit data bus, as illustrated in Figure 2.13. The new PCI specification runs at 66MHz to provide a 264MBps data throughput. The slot also features a reduced 3.3Vdc power supply voltage to decrease signal interference levels generated by the 33MHz operations. Adapters placed in the 32-bit section of the PCI 2.2 slot can operate with the 5Vdc or 3.3V supply levels. The back portion of the slot remains pin- and signal-compatible with the older 32-bit PCI slots. It retained its +5Vdc operating voltage to remain compatible with older PCI 1.1 and 2.0 adapters.

An additional PCI bus improvement has been developed using a new slot layout for PCI 2.3. This slot is similar to the PCI 66-32/64 intermediate slot in size and appearance. However, it is keyed in such a manner that only adapter cards designed for this slot (or universal PCI cards) can be inserted. The slot also features a reduced 3.3Vdc power supply voltage to decrease signal interference levels generated by the 66MHz operations.

PCI Configuration

The PCI standard is part of the PnP hardware standard. As such, the system's BIOS and system software must support the PCI standard. Although the PCI function is self-configuring, many of its settings can be viewed and altered through the CMOS setup utility.

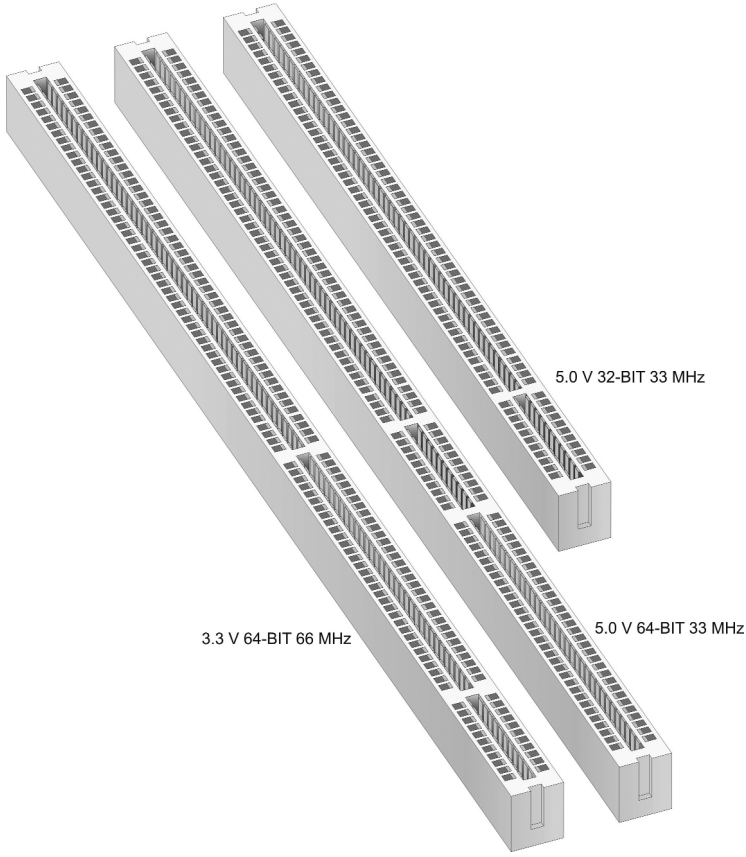


FIGURE 2.13 32-bit and 64-bit PCI slots.

During a portion of the bootup known as the *detection phase*, the PnP-compatible BIOS checks the system for devices installed in the expansion slots to see what types they are, how they are configured, and which slots they are in. For PnP-compatible I/O cards, this information is held in a ROM device on the adapter card.

The BIOS reads the information from all the cards and then assigns each adapter a *handle* (logical name) in the PnP Registry. It then stores the configuration information for the various adapters in the Registry as well.

Next, the BIOS compares the adapter information to the system's basic configuration in search of resource conflicts. After evaluating the requirements of the cards and the system's available resources, the PnP routine assigns system resources to the cards as required.

Because the PnP process has no method for reconfiguring legacy devices during the resource assignment phase, it begins by assigning resources, such as IRQ assignments, to these devices before servicing the system's PnP devices.

Likewise, when the BIOS detects the presence of a new device during the detection phase, it disables the resource settings of its existing cards, checks to determine what resources are required and available, and then reallocates the system's resources as necessary.

EXAM ALERT

Know the process the PnP system employs to allocate resources to a new device in an existing system.

Depending on the CMOS settings available with a particular PCI chipset, the startup procedure may be set up to configure and activate all the PnP devices at startup. With other chipsets, it may also be possible to check all cards, but enable only those actually needed for startup. Some CMOS routines contain several user-definable PCI configuration settings. Typically, these settings should be left in default positions. The rare occasion for changing a PCI setting occurs when directed to do so by a product's installation guide.

Systems may, in theory, contain an unlimited number of PCI slots. Only four slots are included on most system boards because of signal loading considerations. The PCI bus includes four internal interrupt lines (INTa through INTd, or INT1 through INT4) that enable each PCI slot to activate up to four different interrupts. PCI interrupts should not be confused with the system's IRQ channels, although they can be associated with them if required by a particular device. In these cases, IRQ9 and IRQ10 are typically used.

PCI-X

PCI bus versions after PCI 2.3 were given a designation of PCI-X (along with a description of their operating speeds, such as PCI-X 66). These PCI-X specifications are enhanced versions of the 64-bit 66MHz PCI 2.3 bus specification.

- PCI-X 1.0 was based on the previous PCI 2.3 architecture and offers support for 3.3V and universal PCI cards. Therefore, conventional 33/66MHz PCI cards can be used in PCI-X 1.0 slots. Conversely, PCI-X 1.0 cards could be used in standard PCI slots. PCI-X 1.0 provides 66 and 133MHz bus speed options.

- PCI-X 2.0 was derived from PCI-X 1.0 and introduced an Error Correction Code (ECC) feature to improve data transfer reliability. It also introduced two new speed options: PCI-X 266MHz (which provides 2.13GB/sec transfer rates) and PCI-X 533MHz (with 4.26 GB/sec transfer rates).

All the PCI-X versions are backward compatible with the original PCI specifications (that is, they employ the same form factors, pin-outs, connector, 32/64-bit bus widths, and protocols as the original PCI specification). However, the slowest board installed in one of the PCI-X slots determines the operating speed for all the PCI devices. Although these versions offered some improvements over previous PCI versions, they have never been widely used in desktop PCs or network workstations. Instead, boards with these slots have typically been used in more powerful network server computers.

PCI Express

Originally, there was a PCI-X 1066 expansion slot version envisioned. However, as signal speed increases in parallel bus connections, it becomes much more difficult to reliably transmit and receive data. The electrical quantities associated with insulated, parallel conductors eventually outweigh the advantages of sending multiple bits of data at the same time. When this point is reached in any type of communications setting, the answer is always to implement some type of serial (one bit at a time using one communication path) method of moving the information from point A to point B.

The PCI specification shifted to a serial PCI expansion scheme called PCI Express (PCIe). The Pentium/PCIe chipset employs the same software driver support as traditional PCI interfaces. However, under PCIe, the data moving back and forth across the bus is formed into serialized packets before being sent and is then converted back to parallel format after it has been received.

The basic PCIe architecture employs two low-voltage differential signal (LVDS) pairs of data lines that carry data back and forth at rates up to 5.5GBps in each direction. Each two-pair communication path is referred to as a *lane* and is capable of transmitting one byte at a time in both directions at once. This full-duplex communication is possible because each lane is made up of one send and one receive path.

Under the PCIe specification, PCIe switching devices can combine multiple PCIe lanes together to provide additional bandwidth between the PCIe host and the PCIe device. Each complete connection between a host and a device (or slot)

is referred to as a *link*. Figure 2.14 illustrates the relationship between PCIe lanes and links. In this example, two PCIe lanes are routed to a particular PCIe slot configuration to provide a two-lane (×2) link capable of carrying twice as much information as a single-lane link (×1).

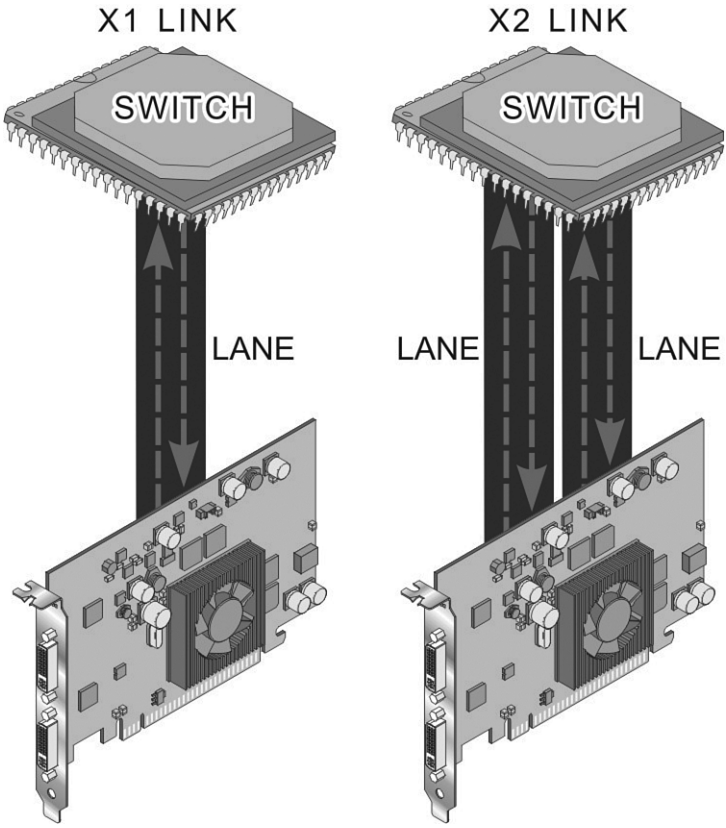


FIGURE 2.14 PCIe lanes and links.

The PCIe specification supports ×1, ×2, ×4, ×8, ×12, ×16, and ×32 lane links. However, available PCIe chipsets provide for only 20 lanes, and 16 are typically used for the ×16 PCIe graphics slot. The PCIe switches depicted in the figure are built into the South Bridge of the chipset and provide links to most of the PCIe expansion slots. In some chipset versions the ×16 slots are connected directly to a PCIe switch in the North Bridge. To date, this slot is the most successful implementation of the PCIe standard. The other four lanes can be distributed between any combination of ×1, ×2, or ×4 slots.

PCIe Slots

PCIe employs four slot connector sizes. The ×1 slot contains 36 contact positions. The ×4 slot is physically larger and has 64 pins, the ×8 version uses 98 pins, and the ×16 has 164 pins. Figure 2.15 shows the different PCIe expansion slots and their pin assignments.

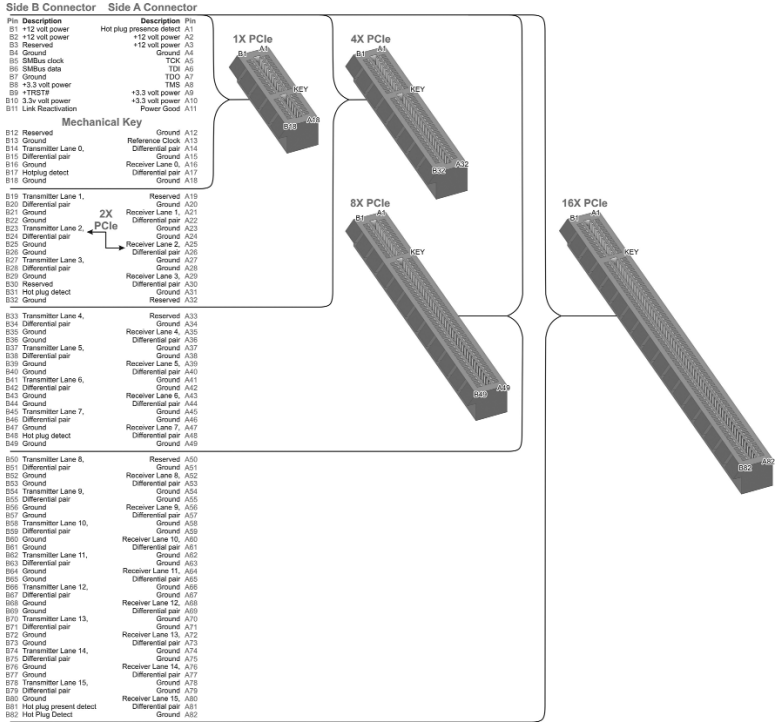


FIGURE 2.15 PCIe slots and pinouts for each.

The number and arrangement of PCIe slots on system boards is largely up to the discretion of the system board manufacturer. The BTX form factor specification calls for one ×16 slot and two ×1 slots for its system boards. The ×16 slot replaces the traditional AGP slot (covered in the next section of this chapter) for the graphic display adapter. Some system boards include two ×16 slots, whereas others offer a mixture of ×8, ×4, and ×1 slots. These system boards may also include some number of traditional PCI slots.

It is permissible to plug PCIe adapter cards with fewer lanes into a larger slot (for instance, a ×8 card into a ×16 slot). The card's edge connector will not fill the slot, but the electrical contact connections should line up properly and the card should function correctly. The PCIe host adapter (known as a *PCIe switch*)

portion of the chipset will automatically assess the card in the slot during start-up and assign the required number of lanes to the slot. The unused lanes are then available for use in other PCIe slots.

System boards designs may include both traditional PCI and PCIe slots. A *PCI-to-PCIe bridge* translates PCIe information into standard PCI signals. This bridging enables standard PCI devices to be included in the PCIe system. The bridging circuitry is starting to be included in PCIe chipsets. On these boards, the PCI bridge is part of the South Bridge device. In other cases, the bridge is included in the adapter card.

PCIe Configuration

During the PnP process, the PCIe switch portion of the chipset negotiates with any PCIe devices to establish the maximum number of lanes available for the link. The outcome of the negotiation depends on three factors:

- The number of physical lanes the link can support
- The number of lanes that the device requires
- The number of lanes the PCIe switch can support

If the device, such as an advanced PCIe video card, contains 16 lanes, it will need to be inserted into an ×16 slot. However, if the device has only 8 lanes, the PCIe switch will detect this and allocate only the 8 lanes required. If the link supports more than 16 lanes, the extra lanes will be ignored.

If the device has more lanes than the link can furnish, the device and the switch throttle back to the number of lanes available. The one situation where this would not be the case is where the physical edge connector does not match the physical connector.

AGP Slots

Many ATX system board designs include an advanced Accelerated Graphics Port (AGP) interface for video graphics. The AGP interface is a variation of the PCI bus design that has been modified to handle the intense data throughput associated with 3D graphics.

EXAM ALERT

Know what type of device is plugged into an AGP slot.

The AGP specification was introduced by Intel to provide a 32-bit video channel that runs at 66MHz in basic 1× video mode. The standard also supports three high-speed modes: 2× (5.33MBps), 4× (1.07GBps), and 8× (2.1GBps).

The AGP standard provides for a direct channel between the AGP graphic controller and the system's main memory, instead of using the expansion buses for video data. This removes the video data traffic from the PCI buses. The speed provided by this direct link permits video data to be stored in system RAM instead of in special video memory. System boards designed for portable systems and single-board systems may incorporate the AGP function directly into the board without using a slot connector.

As illustrated in Figure 2.16, three types of slot connectors have been used to deliver the AGP function for system boards used in desktop and tower units. The system board typically features a single slot that is supported by a Pentium/AGP-compliant chipset. The original slot configuration had a key located toward the rear of the board. These slots were used with 3.3V (2×) adapters.

The second AGP slot version moved the key toward the front of the board, so it was not physically compatible with the older AGP adapters. These slots were used with 1.5 V (4×) adapters. The final revision of the AGP slot is the universal AGP slot that removes all keys so that it can accept any type of AGP card (including universal adapters). These slots can be used with 3.3V, 1.5V, and 0.8V (2×/4×/8×) adapters.

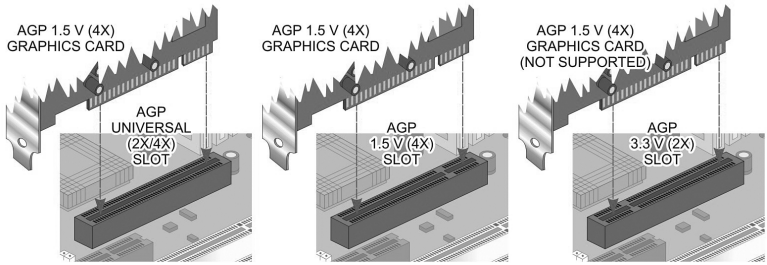


FIGURE 2.16 AGP slots.

The newer 8× specification employs a lower supply voltage (0.8) than the 2× and 4× specifications. When upgrading an AGP card or a system board containing an AGP slot, you should always consult the system board and AGP adapter

card's documentation to verify their compatibility with each other. Usually the Chipset Features page of the CMOS setup utility provides user-configurable AGP slot parameters that can be used to manually configure the adapter's parameters. The default setting for this option is Autodetect. In this mode, the PnP process will detect the card and assign the correct voltages and maximum speed settings for that type of card.

Table 2.2 compares the capabilities of the various bus types commonly found in personal computers. It is quite apparent that the data-transfer rates possible with each new version increase dramatically. The reason this is significant is that the expansion bus is a speed-limiting factor for many of the system's operations. Every peripheral access made through the expansion slots requires the entire computer to slow down to the operating speed of the bus.

TABLE 2.2 Expansion Bus Specifications

BUS TYPE	TRANSFER RATE	DATA BITS	ADDRESS BITS	DMA CHANNELS	INT CHANNELS
ISA	8MBps	16	24	8	11
PCI 2	132/264MBps	32/64	32	None	3
PCI 2.1	264/528MBps	32/64	32	None	3
PCI-X 1.0	1.06GBps	64	64	None	3
PCI-X 2.0	2.13/4.26GBps	64	64	None	3
PCIe	250MBps per lane	Serial	None	None	None
AGP	266/533/1,070MBps	32	32	None	3

EXAM ALERT

You must be able to identify standard expansion slot types from different ATX system board outline drawings.

Audio Modem Risers and Communication Networking Risers

Intel developed an audio/modem standard for system board designs that separates the analog and digital functions of audio (sound card) and modem devices.

This standard includes an expansion slot connection, called the Audio Modem Riser (AMR), and a companion expansion card format, known as the Mobile Daughter Card (MDC). The analog portion of the function is placed on the MDC riser card and the digital functions are maintained on the system board. These components are depicted in Figure 2.17.

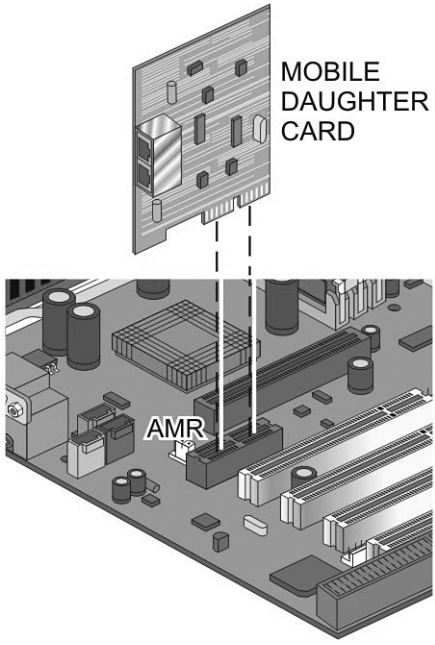


FIGURE 2.17 Audio Modem Riser components.

AMR slots are already being replaced in Pentium systems by a new design called the Communications and Networking Riser (CNR) card, depicted in Figure 2.18. This specification improves on the AMR specification by including support for advanced V.90 analog modems, multichannel audio, telephone-based dial-up networking, and USB devices, as well as 10/100 ethernet-based LAN adapters.

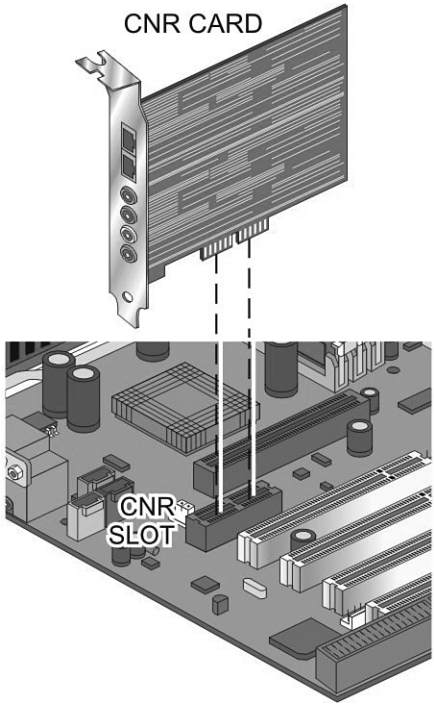


FIGURE 12.18 Communications and Networking Riser card components.

I/O Ports

Many of the PCs standard I/O port circuits have been integrated directly into the system board's chipset and BIOS/CMOS structures. The corresponding hardware ports were grouped into a standardized block of connections in the ATX specification, as illustrated in Figure 2.19. These connectors are placed along the back edge of the system board and extend through the back panel of the system unit. The back panels of specific PCs may have all the connections depicted in the figure, or they may have some subset of these connections.

The panel features two (0.25 inch) 6-pin PS/2 mini-DIN connectors specified for both the mouse and the keyboard. The lower connector is designated for keyboards equipped with PS/2 connectors, and the upper connector is intended for use with a PS/2 mouse. Because these connectors are physically identical, it is relatively easy to confuse them. To compensate for this possibility, manufacturers have color coded these connectors—purple indicates that the connection is for the keyboard, and green is used for the mouse.

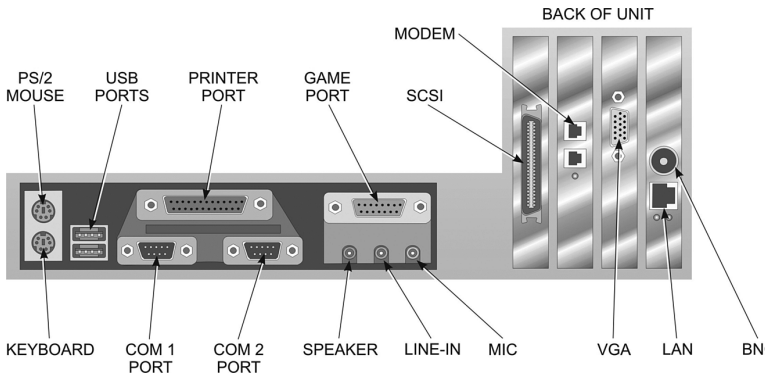


FIGURE 2.19 Standard ATX back panel connections.

To the right of the keyboard and mouse ports is a DB-9M D-shell COM port connector for use with serial devices, a DB-25F D-shell parallel-port connector for SPP, EPP, and ECP parallel devices, and a digital coaxial audio output connector.

Next are two stacks of two USB connectors. An IEEE-1394 FireWire port tops the first stack. These are high-speed serial interface ports that allow various peripheral devices to be attached to the system. The second stack is topped with an RJ-45 connector to accommodate CAT5 local area networking. These connectors are keyed so they cannot be misaligned.

Other integrated I/O ports commonly found on the back of PC systems include additional serial ports, integrated DB-15F D-shell VGA display connectors, and 1/8 inch RCA jacks for speakers, microphones, and line-in sources.

EXAM ALERT

You must be able to identify standard I/O connection types from different ATX/BTX system board drawings by their relative sizes and locations.

Onboard Disk Drive Connections

Pentium system boards provide the system's hard-disk/CD-ROM/DVD drive and floppy-disk drive controller functions and interface connections. There are currently three common disk drive connection interfaces provided on system boards: Parallel Advanced Technology Attachment (PATA) and Serial AT Attachment (SATA) connectors for IDE drives, and (possibly) a FDC interface connection.

PATA and SATA interfaces are designed to serve a particular type of drive that places the bulk of the drive controller circuitry on the disk unit instead of on an adapter card. These drives are referred to as *IDE drives*. The IDE designation was originally used to refer to all ATA devices until the advent of the serial ATA interface. At this point, discussions of IDE drives and their interfaces had to be segmented into terms of parallel and serial ATA drives. Figure 2.20 provides an example of a system board that supplies the system's PATA and SATA host adapter connections, along with the FDC interface connection.

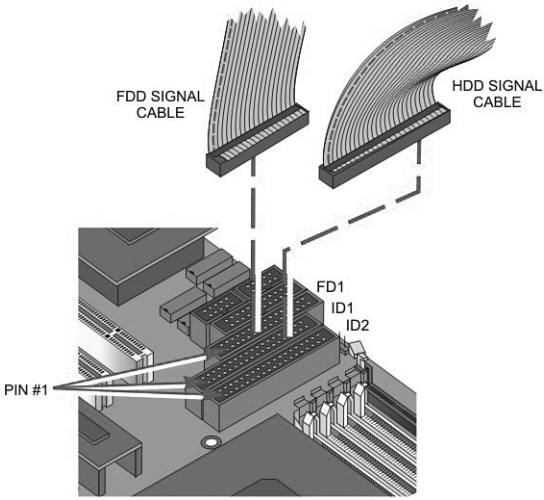


FIGURE 2.20 System board disk drive connections.

The FDC portion of the chipset can control two floppy-disk drives whose signal cable connects to the system board at the 34-pin BERG connector, labeled FD1. As with any disk-drive connections, caution must be taken when connecting the floppy-disk drive signal cable to the system board; pin 1 of the connector must line up with the signal cable's indicator stripe.

PATA Connections

The parallel IDE host adapter portion of the chipset furnishes two complete IDE channels—IDE1 and IDE2—that can handle one master and one slave device each. The IDE hard drives and CD-ROM drives are attached to the system board via signal cables that connect to two 40-pin BERG connectors labeled ID1 and ID2. Traditionally, cables used with internal disk drives have been flat, ribbon cables. However, newer rounded cables are available for connecting disk drives to the system board. The connectors at the ends of the cables are the same, but the rounded cables are supposed to take up less space, provide

better air flow through the case, and be more flexible so they are easier to work with. There are several versions of the PATA/IDE interface. Fortunately, most of these versions are concerned only with the software and drivers that control the flow of information through the interface.

System boards that used the original PATA/IDE specification provided one 40-pin connector on the board and offered a single IDE channel that could control two IDE devices (one master and one slave). Eventually, system boards that support the Enhanced IDE (EIDE) standards for communications and feature two physical IDE connectors were introduced to the market.

Each EIDE channel is capable of handling its own master and slave devices. Over time, the EIDE interface has been redefined to provide faster transfer rates, as well as to handle larger storage capacities. EIDE interfaces can also be used to control drive units such as a tape or CD-ROM. The EIDE interface is often described as an ATAPI (AT Attachment Packet Interface) or a Fast ATA (Fast AT Attachment) interface.

The original PATA/IDE interface employed 40-wire cables between the system board interfaces and the drive units. Of these 40 wires, only 7 were ground wires. As transfer speeds across the PATA cabling increased, the large separation between each signal line and its respective return ground line resulted in decreased reliability over this cable.

For transfer rates greater than 33MHz, the original 40-wire cable was replaced by an 80-wire version that alternates ground and signal lines. This arrangement reduces interference between signal lines, which greatly increased the reliability of each line at higher frequencies. These cables have a maximum length specification of 18 inches.

The 80-wire cables still use the 40-pin IDE connector at each end to remain compatible with standard PATA connections. These cables are typically color coded to prevent them from being confused with older 40-wire cables, which are typically gray. However, when newer EIDE devices are connected to the system using an older 40-conductor cable, they will default to operating speeds compatible with the older IDE standards.

Many PATA cable manufacturers also color code the connectors on their cables to suggest where each connector should be attached in the system. The blue connector is intended to be connected to the system board's PATA interface. The black connector should be connected to the master device and the gray connector is used for a slave device, if one is used on the same IDE channel, as illustrated in Figure 2.21.

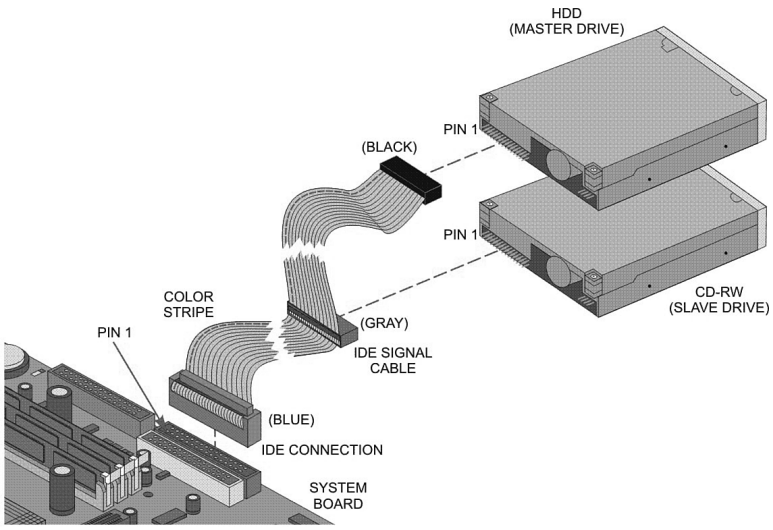


FIGURE 2.21 PATA drive connections.

This color code is just a suggestion—physical configuration jumpers on the devices control the actual designation of master and slave devices. If PATA devices are not connected according to the color code they will still function properly. Procedures for configuring PATA devices are covered in detail in Chapter 7, "Installing, Upgrading, Configuring, and Optimizing PC Components."

Serial ATA Connections

As with all other parallel I/O schemes, the PATA specification eventually ran into performance limitations (speed and distance) associated with parallel transmissions. The SATA interface specification was designed to replace the PATA interface and overcome its electrical constraints. Although it replaces the physical interface connection and cabling structures, the SATA specification remains compatible with the supporting ATA software embedded in existing operating systems.

Figure 2.22 depicts the flat 7-pin SATA signal cable connector and its configuration. Four of the wires are used to form two differential signal pairs (A+/A– and B+/B–), whereas the other three wires are used for shielded grounds. The cable is only 0.5 inches wide. This feature makes cable routing inside the system unit simpler and provides less resistance to airflow through the case. The maximum length for an internal SATA cable is specified as 36 inches (1 meter).

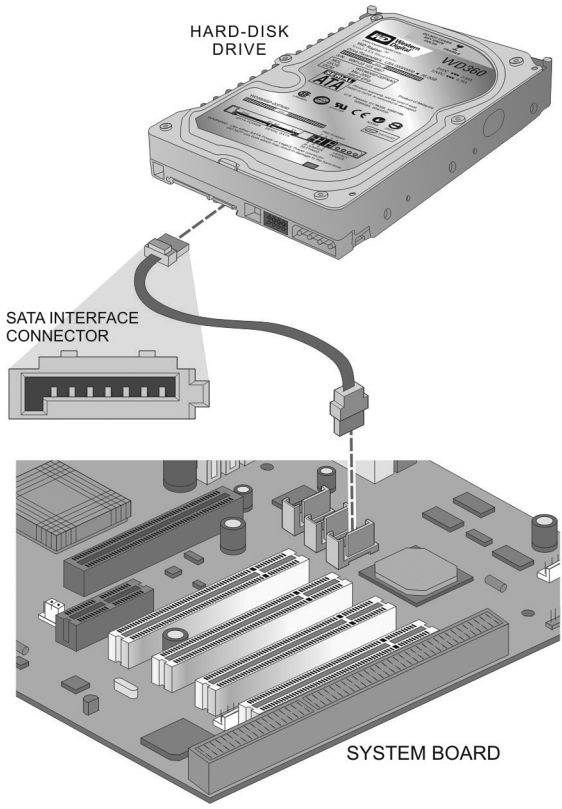


FIGURE 2.22 The Serial ATA interface connector.

Unlike its PATA counterpart, the SATA interface has made provisions for connections outside the system unit case. This type of connection is referred to as the external SATA or eSATA interface. Figure 2.23 illustrates the implementation of a single-lane external SATA interface. An eSATA interface consists of a SATA cable that links the SATA interface on the system board to an eSATA connector on one an expansion slot cover mounted in the rear of the system unit. A shielded eSATA cable is used to connect the drive unit to the slot-mounted interface. The maximum cable length for the external eSATA cable is 6 feet (2 meters).

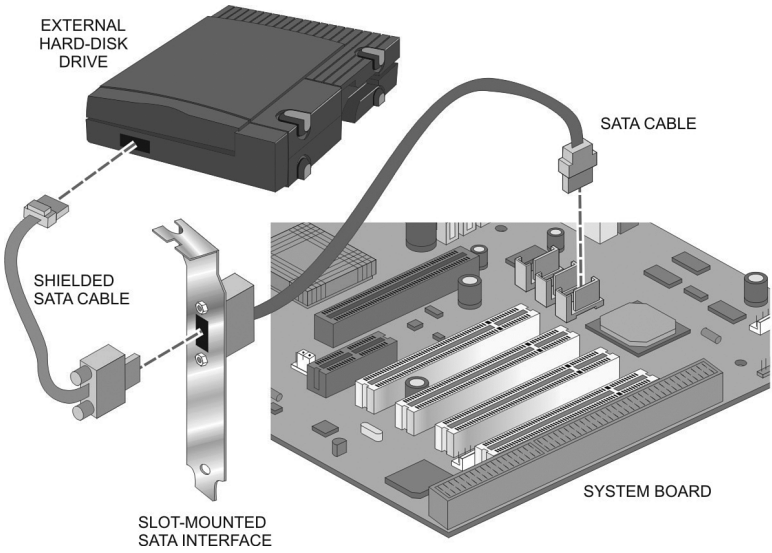


FIGURE 2.23 eSATA interface connections.

SCSI Connections

No industry-accepted equivalents exist for onboard SCSI adapters. Although a few such system board designs are available, they are not standard boards and have probably been created to fill the specific needs of a particular application. Therefore, SCSI devices require that a SCSI host adapter card be installed in most systems.

The built-in SCSI connector on the system board will normally be made through a 50-pin BERG header. Like the IDE drives, support for the onboard SCSI controller must be established through the CMOS setup utility. The system BIOS provides support for the built-in SCSI controller through its CMOS setup utility, whereas add-on adapter cards feature a BIOS extension on the card. Figure 2.24 shows typical SCSI connections.

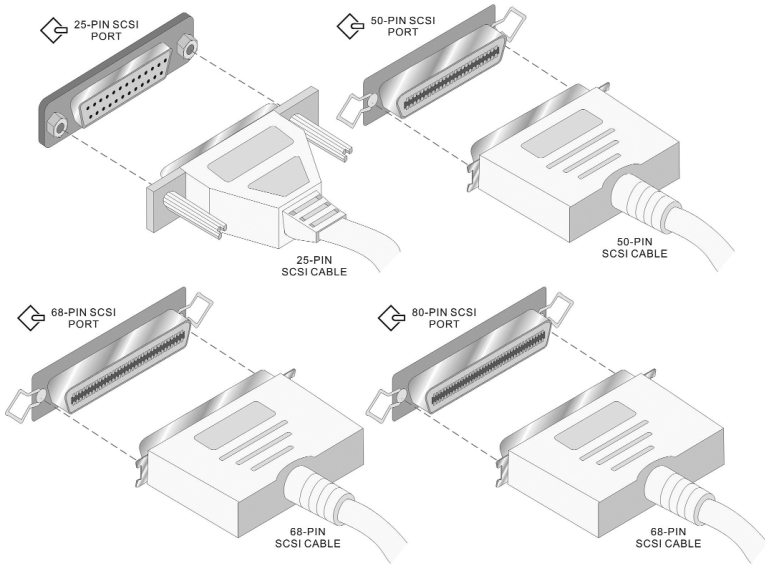


FIGURE 2.24 SCSI connections.

Processor Socket Specifications

Intel has always developed lines of upgrade microprocessors for its original offerings. These are referred to as *OverDrive processors*. An OverDrive unit may be the same type of microprocessor running at a higher clock speed, or it may be an advanced architecture microprocessor designed to operate from the same socket/pin configuration as the original. To accommodate this option, Intel created specifications for eight socket designs, designated Socket 1 through Socket 8.

The specifications for Socket 1 through Socket 3 were developed for 80486SX, 80486DX, and 80486 OverDrive versions that use different pin numbers and power supply requirements. Likewise, the Socket 4 through Socket 6 specifications deal with various Pentium and OverDrive units that have different speeds and power supply requirements.

The Socket 7 specification enabled system boards to be configured for different types and versions of microprocessors using different internal core and FSB operating speeds. Its design includes provision for a Voltage Regulator Module (VRM) to allow various power settings to be implemented through the socket.

The Socket 7 specification corresponds to the second generation of Pentium devices that employ SPGA packaging. It is compatible with the Socket 5, straight-row PGA specification that the first-generation Pentium processors employed. Finally, the Socket 8 specification is specific to the Pentium Pro processor.

An upgraded Socket 7 specification, referred to as Super Socket 7, was developed to extend the use of the Socket 7 physical connector. This upgrade added support signals required for implementing AGP slots and the 100MHz front-side bus (FSB) specification. Microprocessors designed to use the Super Socket 7 specification include AMD's K6-2, K6-2+, and K6-III, along with Intel's Pentium MMX and Pentium Pro.

Although the Intel Slot 1 design was originally developed for the Pentium II, it also serves the Celeron and Pentium III processor designs. Like Socket 7, the Slot 1 specification provides for variable processor core voltages (2.8 to 3.3) that permit faster operation and reduced power consumption. In addition, some suppliers have created daughter boards containing the Pentium Pro processor that can be plugged into the Slot 1 connector. This combination Socket 8/Slot 1 device is referred to as a *slotket processor*.

The Slot 2 specification from Intel expands the Slot 1 SECC technology to a 330-contact (SECC-2) cartridge used with the Intel Xeon processor.

In a departure from its proprietary slot connector development, Intel reversed direction and introduced a new ZIF socket standard, called Socket 370, for use with its Celeron processor. There are two versions of the Socket 370 specification. The first is the PPGA 370 variation intended for use with the Plastic Pin Grid Array (PPGA) version of the Celeron CPUs. The other is the Flip Chip Pin Grid Array (FC-PGA) version.

NOTE

When Intel retreated from the slot processor designs and returned to sockets for its processors, it abandoned the linear socket numbering system and began referring to the socket by its pin count (for example, Socket 370 is a socket that has 370 pins—the company originating the use of the socket gets to specify what each pin represents).

The term *flip chip* is used to describe a group of microprocessors that have provisions for attaching a heat sink directly to the microprocessor die. The processors in this category include the Cyrix III, Celeron, and Pentium III. Although the PPGA and FC-PGA processors will both plug into the 370 socket, that does not mean they will work in system board designs for the other specifications.

The original P4 was delivered in a Socket 423 configuration. Subsequent versions have been produced using Socket 478 or flip chip LGA775 sockets. Intel has continued to employ the LGA775 socket arrangement for a number of its newer processor designs, including

- Pentium 4 (2.66—3.800GHz)
- Celeron D (2.527—3.333GHz)
- Pentium 4 Extreme Edition (3.2GHz, 3.400—3.73GHz)
- Pentium D (2.80—3.40GHz)

Intel has also offered a variety of front-side bus speed options through this socket type, including 133MHz /533FSB, 200MHz /800FSB, 266MHz /1066FSB; and 333MHz/1333FSB speeds. The LGA775 package features 250 power and 273 ground pins to accommodate the processor's 130 watts of power dissipation.

AMD Slots and Sockets

AMD produced a reversed version of the Slot 1 specification for its Athlon processor by turning the contacts of the Slot 1 design around. They titled the new design Slot A. While serving the same ends as the Slot 1 design, the Slot A and Slot 1 microprocessor cartridges are not compatible.

In addition, a 462-pin ZIF socket specification was adopted for the PGA versions of its Athlon and Duron processors. This has been followed by a line of advanced sockets to keep pace with the updated features of the AMD processors:

- Socket 563—Athon XP-M (low power mobile)
- Socket 754—Athlon 64
- Socket 939—Athlon 64/Athlon 64 FX
- Socket 940—Opteron/Athlon 64 FX
- Socket 462/Socket A—Athlon, Duron, Athlon XP, Athlon XP-M, Athlon MP, and Sepron
- Socket AM2 —A 940-pin socket also known as Socket M2, replaces the current Socket 754 and 939 offerings—Athlon 64, Athlon 64 FX, and Athlon 64 X2

- Socket S1—A 638-pin mobile processor socket that replaces the Socket 754 for Athlon 64 mobile processors and future dual core AMD processors.
- Socket F—A 1207-pin socket that replaces the Socket 940 for dual-processor applications

Table 2.3 summarizes the attributes of the various industry socket and slot specifications.

TABLE 2.3 Industry Socket Specifications

NUMBER	PINS	VOLTAGES	MICROPROCESSORS
Socket 1	169 PGA	5V	80486 SX/DXx, DX4 OverDrive
Socket 2	238 PGA	5V	80486 SX/DXx, Pentium OverDrive
Socket 3	237 PGA	5/3.3V	80486 SX/DXx, Pentium OverDrive
Socket 4	237 PGA	5V	Pentium 60/66, 60/66 OverDrive
Socket 5	320 SPGA	3.3V	Pentium 75-133, Pentium OverDrive
Socket 6	235 PGA	3.3V	Never implemented
Socket 7	321 SPGA	VRM (2.5V–3.6V)	Pentium 75-200, Pentium OverDrive
Socket 8	387 SPGA	VRM (2.2V–3.5V)	Pentium Pro
Slot 1	242 SECC/SEPP	VRM (1.5V–2.5V)	Celeron, Pentium II, Pentium III
Slot 2	330 SECC-2	VRM (1.5V–2.5V)	Xeon
Super Socket 7	321 SPGA	VRM (2.0V–3.5V)	AMD K6-2, K6-2+, K6-III, K6-III+, Pentium MMX
Socket 370	370 SPGA	VRM (1.1V–2.5V)	Cyrix III, Celeron, Pentium III
Slot A	242 Slot A	VRM (1.2V–2.2V)	AMD Athlon
Socket A	462 SPGA	VRM (1.2V–2.2V)	AMD Athlon, Duron
Socket 423	423 FC-PGA	VRM (1.7V)	Pentium IV (1.3GHz–2.0GHz)
Socket 478	478 FC-PGA	VRM (1.5V–1.7V)	Pentium IV Xeon (1.4GHz–2.2GHz)
Socket 603	603 INT-PGA	VRM (1.5V–1.7V)	Pentium IV (1.4GHz–2.2GHz)

TABLE 2.3 *Continued*

NUMBER	PINS	VOLTAGES	MICROPROCESSORS
Socket 418	418 INT-PGA	VRM (1.7V)	Itanium/Intel (733MHz–800MHz)
FC-LGA775 (Socket T)	775 LGA	1.2V–1.4V	Pentium 4/Extreme Edition/D; Celeron D
Socket 563	563 microPGA	1.5–1.75V	Athlon XP-M
Socket 754	754 PGA	0.8–1.55V	Athon 64
Socket 939	939 PGA	0.8–1.55V	Athon 64, Athon 64 FX
Socket 940	940 PGA	0.8–1.55V	Opteron, Athon 64 FX

Challenge #1

Your company does not want to replace all of its computers at this time. In fact, what it really wants to do is spend a little money to upgrade all its computers as much as it can now and wait as long as possible to replace them. Because you are the Technical Service Manager, the company has asked you for a plan to upgrade the systems. You know that nearly all the systems in the company are Pentium II 350MHz machines. What is the most current, fastest upgrade you can recommend to your board of directors?

DRAM Sockets

Pentium system boards supply special 168-pin, 184-pin, or 240-pin snap-in sockets to hold the system's SDRAM, DDR-DRAM or DDR2-DRAM DIMMs. The sockets and DIMMs are keyed so that they cannot be plugged in backward. DIMM sockets are quite distinctive in that they are typically arranged side-by-side and may involve between three and four slots. However, they can be located anywhere on the system board.

Some system boards feature a three-DIMM slot arrangement, referred to as a *split-bank arrangement*. When you are working with these boards, you must refer to their user's manual to determine what types of memory can be used because split-bank arrangements use a different specification for DIMM slot 1 than for DIMM slots 2 and 3. The odd slot is usually organized into one bank, whereas the other two slots combine to form the second bank. If you are not careful when populating these slots, you may create a situation in which the system's memory controller cannot access all the installed RAM.

EXAM ALERT

Be aware of situations that will cause the system to "see" less than the actual amount of installed RAM.

Challenge #2

You have been assigned to upgrade the memory in a number of your office's computers. When you open them, you discover that they have a three-slot DIMM arrangement. Also, you cannot locate a system board user's manual for these computers. You install a 128MB DIMM in each slot. When you start the computer, you see from the POST that the system recognizes only 256MB of RAM. What happened to the other 128MB of RAM, and how can you get the system to recognize it?

CMOS RAM

The configuration of every PC-compatible system is controlled by settings established in its CMOS setup utility. Therefore, every technician should be aware of the contents of typical CMOS utilities and be able to properly manipulate the parameters they contain to achieve a fully functional unit and optimize its performance.

CMOS Setup Utilities

The CMOS setup utility can be accessed during the POST process by pressing a designated key. The CMOS setup utility's Main Menu screen, similar to the one depicted in Figure 2.25, appears whenever the CMOS setup utility is engaged. This menu enables the user to select different configuration functions and exit choices. The most used entries include the Standard CMOS Setup, BIOS Features Setup, and Chipset Features Setup options. Selecting these, or any of the other Main Menu options, will lead you into the corresponding submenus.

Other menu items typically include Power Management Setup, PnP/PCI Configuration, Integrated Peripherals, and Password Maintenance Services. The CMOS setup utility of a particular BIOS may contain these same options, or options that perform the same functions under a different name, or it may not contain some of these options at all.

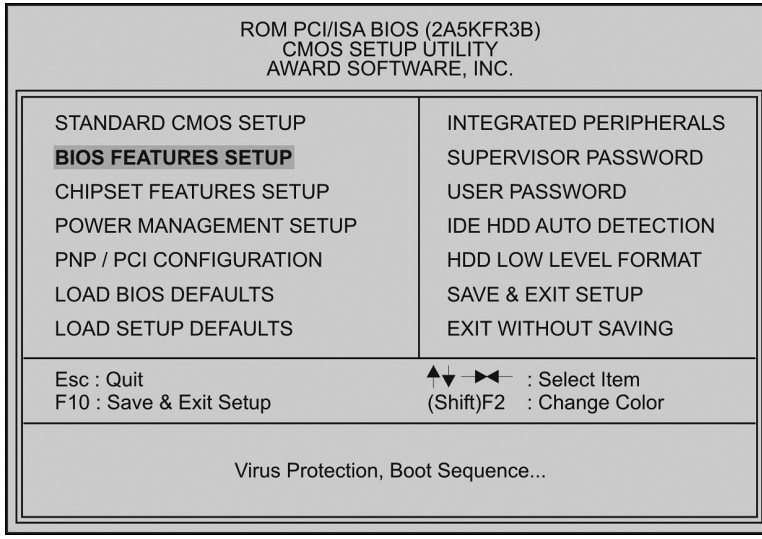


FIGURE 2.25 The CMOS Main Menu screen.

BIOS designers have built two options (Auto Configuration and Default Settings) into newer versions to help users deal with the complexity of the advanced CMOS configuration. Newer system boards use an auto-configuration mode that takes over most of the setup decisions. Working well in most cases, this option produces settings for an efficient, basic level of operation for standard devices in the system. However, it doesn't optimize the performance of the system. To do that, it's necessary to turn off the autoconfiguration feature and insert the desired parameters into the configuration table. Two options typically exist for the autoconfiguration function: Auto Configure with Power-On Defaults and Auto Configure with BIOS Defaults.

The autoconfiguration power-on defaults provide the most conservative system options from the BIOS and the most effective method of detecting BIOS-related system problems. These settings replace any user-entered configuration information in the CMOS setup registers, disabling the turbo speed mode, turning off all memory caching, and setting all wait states to maximum, thus enabling the most basic part of the system for starting.

If these default values fail to boot the system, it indicates possible hardware problems such as incorrect jumper settings or bad components.

If you have entered an improper configuration setting and cannot determine which setting is causing the problem, using the autoconfiguration with the BIOS defaults provides more flexibility than the power-on option. This selection also

replaces the entered configuration settings with a new set of parameters from the BIOS and likely gets you back into the CMOS setup screen so that you can track down the problem. This is also the recommended starting point for optimizing the system's operation.

CAUTION

Set Values with Caution The settings in these menus enable the system to be configured and optimized for specific functions and devices. The default values are generally recommended for normal operation. Because incorrect setup values can cause the system to fail, you should change only setup values that really need to be changed. If changes are made that disable the system, pressing the Insert key on reset will override the settings and start the system with default values.

The standard CMOS setup screens from various BIOS manufacturers all provide the same basic information. They can be used to set the system clock/calendar, establish disk-drive parameters and video display type, and specify which types of errors will halt the system during the POST.

Time and Date

PC chipsets include a Real-Time Clock (RTC) function that keeps track of time and date information for the system. During the startup process, the operating system acquires the time and date information from the CMOS RTC module. This information is updated in the system once every second.

The CMOS uses military time settings (for example, 13:00:00 = 1 p.m.). The PgUp and PgDn keys are used to change the setting after it has been selected using the arrow keys. Most BIOS versions support daylight saving time by adding an hour when daylight saving time begins and subtracting it when standard time returns.

All system boards employ a rechargeable battery to maintain the system's configuration information when it is turned off. In newer systems, the most common battery type is a replaceable 2032 coin cell battery. These are plentiful and easy to change if they become defective. However, in other systems there are no rechargeable batteries for the CMOS storage. Instead, the CMOS storage area and RTC functions have been integrated with a 10-year nonreplaceable lithium cell in an independent RTC IC module.

If the power source or the backup battery becomes defective, the system's capability to keep proper time and date information will be impaired. On older system boards, the backup battery was completely responsible for maintaining the information in the RTC. With newer systems, there is a 5Vdc level present on

the system board even when the system is turned off. On these boards, the power supply and the battery in the RTC module work together to keep the time and date information correct.

If the time is incorrect on a PC system, the easiest way to reset it is through the operating system; however, if the system continually fails to keep good time, you should replace the battery. If that doesn't work, check for corrosion on the battery contacts. Clean the contacts with a pencil eraser and retry the battery. Next, you should try replacing the RTC module. If this does not correct the timekeeping problem, the electronic circuitry that recharges the battery may be defective, and in this case you need a new motherboard.

EXAM ALERT

Be aware of where to go to reset the system clock and what to check if the clock fails to keep proper time.

Disk Drive Support

Most BIOSs possess autodetect options that automatically detect the type of hard drives installed in the system and load their parameters into the CMOS. However, they also provide an entry for user-definable drive settings. Systems with PATA drive capabilities support up to four IDE drives. In older BIOS versions, the CMOS typically did not display information about CD-ROM drives or SCSI devices; however, newer versions show both types of devices when running in autodetect mode.

When the Auto Detect selection is chosen, the BIOS attempts to detect IDE devices in the system during the POST process and to determine the specifications and optimum operating modes for those devices. The drive specifications can also be selected from a built-in list of drive parameters, or they can be entered directly using the User option at the end of the list.

Four translation modes can be selected for each drive type: Auto, Normal, Large, and LBA. In Auto mode, the BIOS attempts to determine the best operating mode for the drive. In Normal mode, the BIOS will support a maximum Cyl/Hds/Sec (CHS) setting of 1024/16/63.

For larger drives (greater than 1,024 cylinders or 504MB), the Large and LBA modes are used. The Large option can be used with large drives that do not support logical block addressing (LBA) techniques. For drives that do support logical block addressing, the LBA mode should be selected. In this mode, the IDE controller converts the sector/head/cylinder address into a physical block address that improves data throughput. Care must be taken when changing the

translation mode setting in CMOS because all data on the drive can be lost in the process.

In the case of errors detected during the POST process, some BIOSs can be set up to halt on different types of errors or to ignore them and continue the boot-up process. These settings include

- No Errors—The POST does not stop for any errors.
- All Errors—The POST stops for all detected errors and prompts the user for corrective action.
- A series of "All But" options—The POST stops for all errors except those selected (that is, all but disk or keyboard errors).

Finally, the screen displays the system's memory usage. The values displayed are derived from the POST process and cannot be changed through the menu. The BIOS displays the system's total detected RAM, base memory, extended memory, and other memory (between the 640kB and 1MB marks). In most CMOS displays, the total memory does not equal the summation of the base and extended memory. This is because the BIOS reserves 384kB for shadowing purposes. Newer BIOS versions may show only the total installed system memory.

Advanced BIOS Features Setup Screen

The Advanced BIOS Features Setup screen provides access to options that extend the standard BIOS functions. Many BIOSs include a built-in virus warning utility that produces a warning message whenever a program tries to write to the boot sector of an HDD partition table. If a warning message is displayed under normal circumstances, a full-featured antivirus utility should be run on the system.

CAUTION

The virus warning utility should be enabled for normal operations; however, it should be turned off when you conduct an upgrade to the operating system. The built-in virus warning utility checks the drive's boot sector for changes. The changes that the new operating system will attempt to make to the boot sector will be interpreted as a virus, and the utility will act to prevent the upgrade from occurring.

EXAM ALERT

You should know that BIOS virus-detection functions should be disabled when performing an operating system upgrade.

This screen is used to configure different bootup options. These options include establishing the system's bootup sequence. Most BIOS versions typically provide user-definable boot sequences for up to four devices. The most commonly used sequence checks the first hard drive as the first boot source. Newer BIOS versions can be configured so the system checks the CD-ROM drive for a boot sector first. You should enable the CD-ROM as the primary boot option when you are installing an operating system or when the system will not boot from the HDD. In these cases, the operating system CD can be used to start the system for installation or troubleshooting purposes.

EXAM ALERT

Know the possible disk seek configuration possibilities and be aware of how they might affect the system in different circumstances.

Challenge #3

Your system will not boot up to the hard drive, so you place a bootable CD-ROM in the drive and try to restart the system. You watch the startup sequence closely and discover that the system does not appear to check the CD-ROM drive for a disc. What should you do to get the system to look for a disc in the CD-ROM drive as part of the bootup activities?

Advanced Chipset Features Setup Functions

The Advanced Chipset Features screen contains advanced setting information that system designers and service personnel use to optimize the chipset. The options and submenus associated with this page can vary greatly from chipset to chipset. The options that you can configure here depend on the functions the chipset provides (for example, FSB options, processor speed/voltage options, AGP configurations, thermal throttling, memory timing options, and so on).

The Auto Configuration option selects predetermined optimal values for the chipset to start with. When this feature is enabled, many of the screen's fields are not available to the user. When this setting is disabled, the chipset's setup parameters are obtained from the system's CMOS RAM. Many of the system's memory configuration parameters are established in this screen.

PnP/PCI Configuration Functions

In most newer PCs, the BIOS, the peripheral devices, and the operating system employ Plug and Play technology that enables the system to automatically

determine what hardware devices are installed in the system and allocate system resources to those devices as required to configure and manage them. This removes some of the responsibility for system configuration from the user or the technician. All three of the system components listed previously must be PnP-compliant before automatic configuration can be carried out.

The BIOS holds information about the system's resource allocations and supplies it to the operating system as required. This information can be displayed through the CMOS PnP/PCI Configuration screen. The operating system must be PnP-compatible to achieve the full benefits of the PnP BIOS. In most PCs, the standard operating system is Windows 2000 or Windows XP, which are both PnP-compliant.

Basically, the PnP device communicates with the BIOS during the initialization phase of the startup to tell the system what type of device it is, where it is located in the system, and what its resource needs are. This information is stored on the device in the form of firmware. The BIOS stores the PnP information it collects from the devices in a special section of the CMOS RAM known as the Extended System Configuration Data (ESCD) area. This information is stored in the same manner as standard BIOS settings are stored.

The BIOS and operating system both access the ESCD area each time the system is restarted to see if any information has changed. This enables the BIOS and the operating system to work together in sorting out the needs of the installed devices and assigning them needed system resources.

EXAM ALERT

Know which portion of the BIOS is responsible for implementing the PnP process.

If no changes have occurred in the contents of the ESCD since the last startup occurred, the BIOS will detect this and skip that portion of the boot process. When a PnP operating system checks the ESCD to see if any hardware changes have occurred, it will react accordingly and record any changes it finds in the hardware portion of its Registry. On some occasions, the system's PnP logic may not be able to resolve all of its resource needs, and a configuration error will occur. In these cases, the technician or the user will have to manually resolve the configuration problem. The BIOS and the operating system typically provide interfaces to the hardware configuration information so that users can manually override the system's PnP resource assignments.

Challenge #4

Your local area network connection to the Internet crashes often and tends to be down for some time. For these occasions you want to establish a dial-up connection to the Internet from your office computer. Your boss does not want to buy a new PnP modem for your use. However, you have an old internal ISA modem in your desk drawer and want to install it in your system to perform this function through your office phone connection. What do you have to do to make this modem work in your plug-and-play system?

Integrated Peripherals Setup Functions

In most Pentium-based systems, the standard I/O functions are configured through the BIOS Integrated Peripherals screen, depicted in Figure 2.26. This screen provides configuration and enabling settings for the system board's IDE drive connections, floppy-disk drive controller, onboard UARTs, and onboard parallel port.

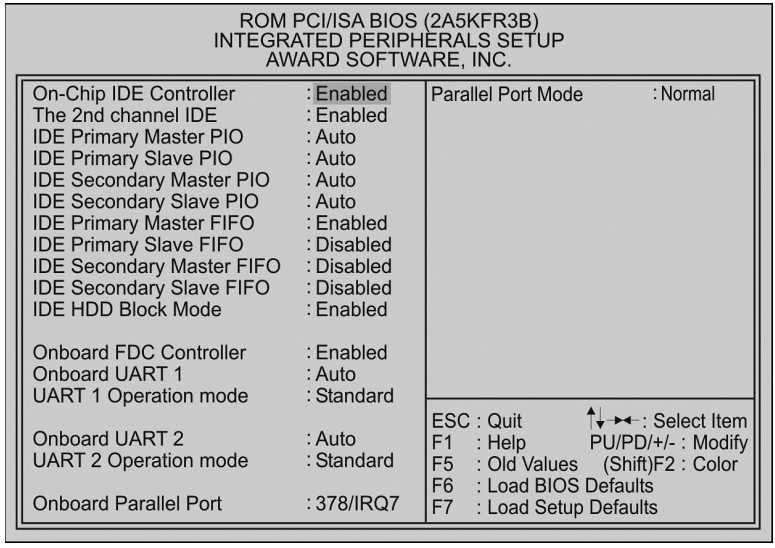


FIGURE 2.26 The Integrated Peripherals screen.

IDE Functions

The Integrated Peripherals screen is used to enable the onboard IDE controller. As mentioned earlier, the second IDE channel can be enabled or disabled independently of the first channel, provided that the controller has been enabled.

Any of the four possible devices attached to the interface can be configured for master or slave operation.

The system's SATA drives and their operating modes are also enabled and configured through the CMOS setup utility. You can typically select among enabling the PATA interface controller, the SATA interface controller, or both. Because the SATA controller is an integral part of the IDE subsystem, you may see options for enabling up to six IDE devices in the CMOS Setup utility. The IDE rules still apply to the four PATA devices in the system.

The IDE HDD Block Mode selection should be set to Enabled for most new hard drives. This setting (also referred to as *Large Block Transfer*, *Multiple Command*, and *Multiple-Sector Read/Write* mode), supports LBA disk-drive operations. If the Auto mode option is selected, the system will determine which mode is best suited for each device.

Implementing Ports

The other onboard I/O functions supported through the CMOS utility can include enabling/disabling the FDD controller, enabling and configuring the system's onboard USB and IEEE-1394 FireWire ports, selecting the logical COM port addressing and operating modes for the system's two built-in UARTs, and selecting logical addressing and operating modes for the parallel port. Other onboard functions configured through this screen include onboard audio and local area networking interfaces, as well as built-in support for game ports and MIDI music ports, on those system boards that offer them.

All newer PCs rely on high speed USB and/or IEEE-1394 ports as their major I/O connections. The controller functions for these ports are typically integrated into the system board's chipset circuitry. They are also enabled/disabled through its CMOS setup utility.

If the system supports a legacy serial communications port, the chipset includes a UART device that can be configured to support half-duplex or full-duplex transmission modes for dialup networking, or to support an infrared communications port, provided the system board is equipped with one. This port enables wireless communications with serial peripheral devices over short distances.

The parallel printer port can be configured for Standard Parallel Port (SPP) operation, for extended bidirectional operation (Enhanced Parallel Port, or EPP), for fast, buffered bidirectional operation (Extended Capabilities Port, or ECP), or for combined ECP+EPP operation. The normal CMOS setting should be selected unless both the port hardware and driver software support EPP and/or ECP operation.

EXAM ALERT

Remember that ECP and EPP modes for the parallel port must be enabled through the CMOS setup utility.

Enhanced Parallel Port Operations

When EPP mode is selected in the port's configuration register, the standard and bidirectional modes are enabled. The functions of the port's pins are redefined under the EPP specification. When the EPP mode is enabled, the port can operate either as a standard, bidirectional SPP parallel port, or as a bidirectional EPP port. The software controlling the port will specify which type of operation is required.

The ECP mode provides a number of advantages over the SPP and EPP modes. In particular, it offers higher performance than either of the other modes. As with the EPP mode, the pins of the interface are redefined when ECP mode is selected in the system's CMOS. The ECP port is compatible with the standard LPT port and is used in the same manner when no ECP operations are called for. However, it also supports high-throughput DMA operations for both forward- and reverse-direction transfers.

Because both of the advanced parallel port modes operate in a bidirectional, half-duplex manner, they require an IEEE-1284-compliant cable. Standard parallel cables designed for older SPP operations may not support these qualities.

EXAM ALERT

Be aware that a non-IEEE-1284 rated parallel printer cable should not be used with bidirectional EPP or ECP devices.

Infrared Port Operation

Infrared Data Association (IrDA) ports provide short-distance wireless connections for different IrDA-compliant devices, such as printers and personal digital assistants. Because the IrDA port communicates by sending and receiving a serial stream of light pulses, it is normally configured to work with the UART of the system's second serial port. This arrangement is established through the Integrated Peripherals page of the CMOS setup utility. In this manner, the infrared port is assigned the system resources that are usually reserved for the COM2/COM4 serial ports.

To enable the IrDA port, the mode for the COM2 UART must be set to automatic and one of the infrared protocol settings (HPSIR or ASKIR) must be

selected. In addition, the transmission duplex mode must be selected (usually half duplex). The operations of the infrared port and the second serial port are mutually exclusive. When the Infrared option is enabled in CMOS, the second serial port will be disabled.

Challenge #5

A customer brings in a computer that has a laser printer and a scanner connected to the parallel port. The scanner is connected directly to the computer's parallel port and the printer is connected to the scanner. The customer cannot get the scanner to work, but the printer operates correctly. What two actions should you perform to determine why the scanner does not work correctly?

Power Management Functions

The Power Management fields enable the user to select from different power saving modes: Doze, Standby, Suspend, or Hibernate. These are green PC-compatible power-saving modes that step the system incrementally down from maximum power usage. The Doze setting causes the microprocessor clock to slow down after a defined period of inactivity. The Standby mode shuts down the hard drive and video after a period of inactivity. Everything in the system except the microprocessor shuts down in Suspend mode. Certain system events, such as IRQ and DRQ activities, cause the system to wake up from these modes and resume normal operation. In Hibernate mode, the system saves the current information in memory to the hard disk drive and shuts down. When the system is restored form Hibernate mode, the environment is returned to the state it was in when Hibernate mode was initiated.

PC Health Status

The PC Health menu, shown in Figure 2.27, displays status information for the critical elements of the system board, including the microprocessor temperature, fan speeds, and actual voltage levels. The page also enables you to establish set points for issuing notifications and alarms when these variables are outside of the desired ranges of operation.

Temperature monitoring can be as simple as tracking the microprocessor's package temperature, or it can include monitoring the case temperature in multiple locations. Key voltage levels tracked by the BIOS include the microprocessor core voltage, the expansion slot voltages, and the various voltage levels being provided to the system board by the power supply.

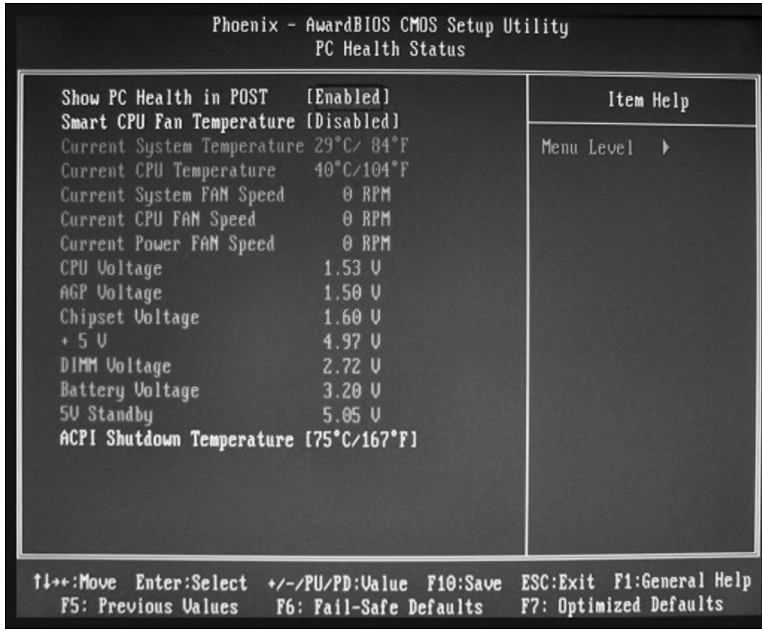


FIGURE 2.27 The PC Health Menu screen.

Finally, this screen enables you to establish warning and system shut down levels that will either warn the user that something is going wrong, or will go ahead and shut the system down to protect the microprocessor from harm.

Security Subsystem

Most BIOSs offer a variety of security options that can be set through the CMOS setup utility. Figure 2.28 displays a typical Security Configuration screen. Typically, these options include setting User passwords to control access to the system and Supervisory passwords to control access to the CMOS setup utility. The User password option enables administrators to establish passwords that users must enter during the startup process to complete the boot process and gain access to the operating system. However, this password does not provide access to the CMOS setup utility. The Supervisory password option establishes a password that must be used to access the CMOS setup utility (where the User and Supervisory password options are configured).

EXAM ALERT

Be aware of the types of passwords that can be established through the CMOS Setup utility.

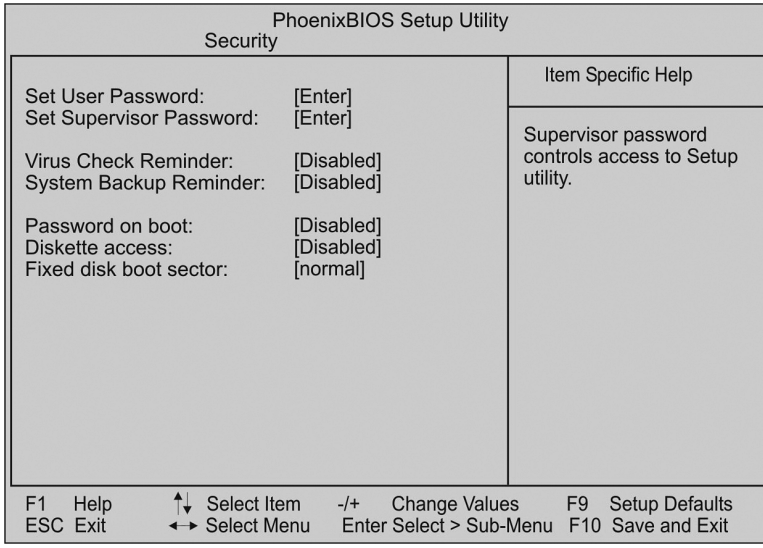


FIGURE 2.28 The CMOS Security configuration.

The Security Configuration screen may also include options for setting virus check and backup reminders that pop up periodically when the system is booted. In addition to enabling these settings, administrators can also specify the time interval between notices.

One of the main sets of security options in the CMOS setup utility consists of those that can be used to control access to the system. For the most part, these options cover such things as access permitted through the floppy drive and access to the boot sector of the drive.

Because the CMOS password controls access to all parts of the system, even before the bootup process occurs, there is some inconvenience in the event that the user forgets a password. When this occurs, it will be impossible to gain access to the system without completely resetting the content of the CMOS RAM. On some system boards, this can be accomplished by shorting a special pair of jumpers on the board.

With other systems, you will need to remove or short across the backup battery to reset the CMOS information. It will also be necessary to unplug the power from the commercial outlet to reduce the voltage to the CMOS registers. When the content of the CMOS is reset, you must manually restore any nondefault CMOS settings being used by the system.

EXAM ALERT

Be aware of the effects of forgetting a CMOS password and know what steps must be taken to restore the system in this event.

Exam Prep Questions

1. What type of expansion bus is based on a 124-pin slot?

   - ❍ **A.** ISA
   - ❍ **B.** PCI
   - ❍ **C.** AGP
   - ❍ **D.** PC-bus

2. Which IRQ resources are assigned in the PnP configuration process?

   - ❍ **A.** Motherboard devices
   - ❍ **B.** ISA devices
   - ❍ **C.** PCI devices
   - ❍ **D.** Legacy devices

3. What type of expansion card is plugged into an AGP slot?

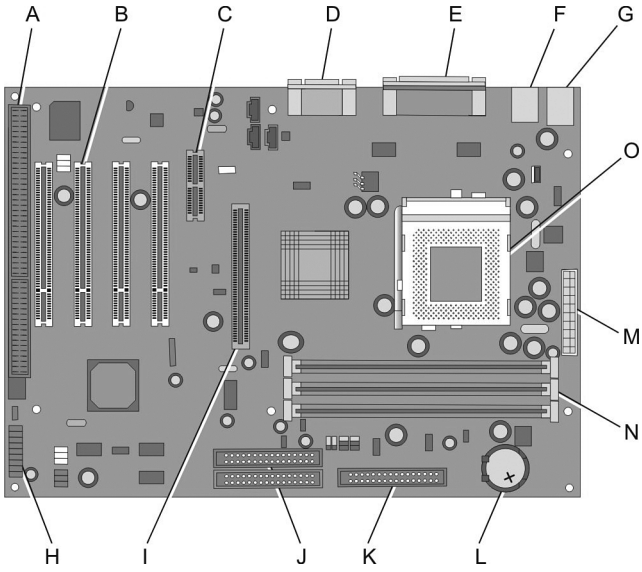
   - ❍ **A.** Graphics
   - ❍ **B.** Modem
   - ❍ **C.** Network
   - ❍ **D.** Sound

4. What is the maximum data throughput when connecting an Ultra ATA 66 hard-disk drive with a 40-pin IDE cable?

   - ❍ **A.** 10Mbps
   - ❍ **B.** 33Mbps
   - ❍ **C.** 66Mbps
   - ❍ **D.** They will not work together.

5. From the figure depicting an ATX motherboard, identify the ISA expansion slot.

- ❍ **A.** A
- ❍ **B.** B
- ❍ **C.** C
- ❍ **D.** D



6. From the figure depicting an ATX motherboard shown in question 5, identify the AGP expansion slot.

- ❍ **A.** A
- ❍ **B.** B
- ❍ **C.** I
- ❍ **D.** N

7. From the figure depicting an ATX motherboard shown in question 5, identify the IDE connectors.

- ❍ **A.** C
- ❍ **B.** J
- ❍ **C.** K
- ❍ **D.** M

8. From the figure depicting an ATX motherboard shown in question 5, identify the battery.

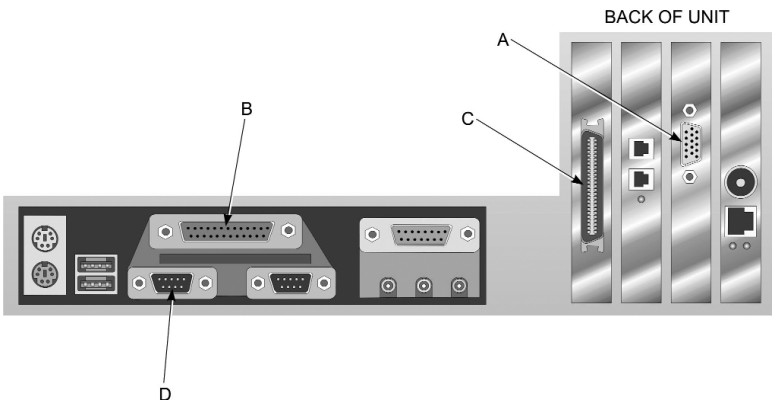
- ❍ **A.** G
- ❍ **B.** H
- ❍ **C.** L
- ❍ **D.** O

9. From the figure depicting an ATX motherboard shown in question 5, identify the DIMM slots.

- ❍ **A.** B
- ❍ **B.** I
- ❍ **C.** H
- ❍ **D.** N

10. Locate the serial port connector in the diagram of an ATX back panel.

- ❍ **A.** A
- ❍ **B.** B
- ❍ **C.** C
- ❍ **D.** D



11. From the figure depicting an ATX back panel shown in question 10, locate the printer port.

- ❍ **A.** A
- ❍ **B.** B
- ❍ **C.** C
- ❍ **D.** D

12. What should you do first if the system clock fails to keep proper time after being reset by the operating system?

- ❍ **A.** Reload the operating system
- ❍ **B.** Replace the battery
- ❍ **C.** Clean the battery contacts
- ❍ **D.** Replace the motherboard

13. What may happen when you change the translation mode setting for an existing IDE drive?

- ❍ **A.** Loss of all data on the drive
- ❍ **B.** Access limited to the first 504MB of the drive
- ❍ **C.** Slower drive access times
- ❍ **D.** Deletion of the MBR

14. Which CMOS functions should be disabled when performing an operating system upgrade?

- ❍ **A.** EPP and ECP
- ❍ **B.** PnP resource allocation
- ❍ **C.** BIOS virus-detection functions
- ❍ **D.** RAM memory checks

15. When your computer boots, you want it to search for a boot sector on a floppy, a CD-ROM drive, and then the hard disk drive. What boot sequence should you set in CMOS?

- ❍ **A.** A, C, SCSI
- ❍ **B.** A, C, CD-ROM
- ❍ **C.** CD-ROM, A, C
- ❍ **D.** A, CD-ROM, C

16. During which portion of the startup process does the BIOS communicate with the system's PnP devices?

- ❍ **A.** During the POST
- ❍ **B.** During the initialization phase
- ❍ **C.** During the OS bootstrap operation
- ❍ **D.** During the CMOS configuration process

17. Which utility must be used to enable the ECP and EPP modes for the parallel port?

- ❍ **A.** DMA setup
- ❍ **B.** CMOS setup
- ❍ **C.** Printer driver
- ❍ **D.** BIOS initialization

18. What types of devices can be used with a half-duplex/bidirectional parallel printer cable? (Select all that apply.)

- ❍ **A.** USB devices
- ❍ **B.** SPP devices
- ❍ **C.** EPP devices
- ❍ **D.** ECP devices

19. What are the effects of forgetting a CMOS password?

- ❍ **A.** You cannot start the computer.
- ❍ **B.** You cannot boot to the operating system.
- ❍ **C.** You cannot log in to the computer.
- ❍ **D.** You cannot shut down the computer.

20. What action must be taken to restore the system if the CMOS password is forgotten in an ATX system?

- ❍ **A.** Change the Password Enable setting in CMOS
- ❍ **B.** Remove the battery
- ❍ **C.** Short the CMOS-enabling jumper and remove the battery
- ❍ **D.** Unplug the computer from the wall and remove the battery

21. Where is the PnP information stored in the BIOS?

- ❍ **A.** The RTC module
- ❍ **B.** The ESCD area
- ❍ **C.** The PnP Registry
- ❍ **D.** The Device Manager

22. The system's time and date configuration can be performed in the _____.

- ❍ **A.** Memory cache
- ❍ **B.** North Bridge
- ❍ **C.** CMOS setup
- ❍ **D.** South Bridge

23. What is the major difference between EPP and ECP operation of the parallel port?

- ❍ **A.** DMA mode
- ❍ **B.** Bidirectional
- ❍ **C.** 16-bit transfers
- ❍ **D.** Serial transfers

24. Which parallel port type has the highest throughput?

- ❍ **A.** ECP
- ❍ **B.** EPP
- ❍ **C.** XPP
- ❍ **D.** SPP

25. What type of communication is possible with an IEEE-1284 parallel cable?

- ❍ **A.** Bidirectional, half-duplex
- ❍ **B.** Bidirectional, full-duplex
- ❍ **C.** Simplex
- ❍ **D.** Selectable half- or full-duplex

26. If you place a bootable floppy in drive A: and the system boots to drive C:, what action should you take to correct this?

- ❍ **A.** Reconfigure the drive seek sequence in the operating system Control Panel
- ❍ **B.** Reconfigure the drive seek sequence in the CMOS setup utility
- ❍ **C.** Disconnect the IDE cable to the drive to force the system to boot from the floppy drive
- ❍ **D.** Reconfigure the floppy jumpers to make it a bootable drive

27. What type of BIOS password should be set on machines that are open to public use?

- ❍ **A.** User access
- ❍ **B.** Remote Access
- ❍ **C.** Admin
- ❍ **D.** Supervisory

28. You are responsible for computers in your area of the building. You need to secure them so that only your employees can access the systems but they cannot change CMOS settings. What type of CMOS password should you set for these machines?

- ❍ **A.** User access
- ❍ **B.** Remote Access
- ❍ **C.** Admin
- ❍ **D.** Supervisory

29. Where should you establish an Administrators password on a computer that will be installed in an Internet cafe?

- ❍ **A.** In the CMOS setup utility.
- ❍ **B.** In the BIOS.
- ❍ **C.** In Windows.
- ❍ **D.** If you set a password in this environment, users will not be able to access the system.

Answers and Explanations

1. B. The PCI bus specification uses multiplexed address and data lines to conserve the pins of the basic 124-pin PCI connector.
2. D. Because the PnP process has no method for reconfiguring legacy devices during the resource assignment phase, it begins by assigning resources, such as IRQ assignments, to these devices before servicing the system's PnP devices.
3. A. The AGP interface is a variation of the PCI bus design that has been modified to handle the intense data throughput associated with three-dimensional graphics.
4. B. All Ultra ATA versions support 33.3MBps data rates when used with a standard 40-pin/40-conductor IDE signal cable.
5. A. Refer to Figures 2.1. For more information, see the section "ATX System Boards."
6. C. Refer to Figure 2.1. For more information, see the section "ATX System Boards."
7. B. Refer to Figure 2.1 An ATX Pentium system board. Along with the I/O port connections, Pentium system boards moved the hard- and floppy-disk drive controller functions and interface connections to the system board. For more information, see section "ATX System Boards
8. C. Refer to Figure 2.1 An ATX Pentium system board. For more information, see the section "ATX System Boards."
9. D. Refer to Figure 2.1 An ATX Pentium system board. For more information, see the section "ATX System Boards."
10. D. Refer to Figure 2.18 Standard ATX back panel connections. For more information, see the section "I/O Conenctions."
11. B. Refer to Figure 2.18 Standard ATX back panel connections. For more information, see the section "I/O Ports."
12. C. If the time is incorrect on a PC system, the easiest way to reset it is through the operating system; however, if the system continually fails to keep good time, you should start by checking for corrosion on the battery contacts. Clean the contacts with a pencil eraser and retry the battery. If that doesn't work, try replacing the battery. Next, you can try replacing the RTC module. If this does not correct the timekeeping problem, the electronic circuitry that recharges the battery may be defective, and in this case you will need a new motherboard.
13. A. Care must be taken when changing the disk drive translation mode setting in CMOS because all data on the drive can be lost in the process.
14. C. BIOS antivirus functions should be turned off when conducting an upgrade to the operating system. The built-in virus warning utility checks the drive's boot sector for changes. The changes that the new operating system will attempt to make to the boot sector will be interpreted as a virus, and the utility will act to prevent the upgrade from occurring.

15. D. The BIOS Features Setup screen is used to configure different bootup options. These options include establishing the system's bootup sequence. The sequence can be set so that the system checks the floppy drive (A:) for a boot sector first, or so that it checks the hard drive (C:) without checking the floppy drive. Other boot options include CD-ROM drives or a SCSI drive.

16. B. The PnP device communicates with the BIOS during the initialization phase of the startup to tell the system what type of device it is, where it is located in the system, and what its resource needs are.

17. B. One of the onboard I/O functions supported through the CMOS Setup utility includes selecting the operating modes for the parallel port. The parallel printer port can be configured for normal PC-AT-compatible standard parallel port (SPP) operation, for extended bidirectional operation (extended parallel port, or EPP), for fast, buffered bidirectional operation (extended capabilities port, or ECP), or for combined ECP+EPP operation. The normal setting should be selected unless both the port hardware and the driver software support EPP and/or ECP operation.

18. C, D. Because both of the advanced parallel port modes (EPP and ECP) operate in a bidirectional, half-duplex manner, they require an IEEE-1284-compliant cable. Standard parallel cables designed for older SPP operations may not support these qualities.

19. B. Because the CMOS password controls access to all parts of the system, even before the bootup process occurs, there is some inconvenience in the event that the user forgets his or her password. When this occurs, it will be impossible to gain access to the system without completely resetting the content of the CMOS RAM.

20. D. On some system boards, resetting the content of the CMOS can be accomplished by shorting a special pair of jumpers on the board. With other systems, you will need to remove or short across the backup battery to reset the CMOS information. In ATX systems, it will also be necessary to unplug the power from the commercial outlet to reduce the voltage to the CMOS registers. When the content of the CMOS is reset, you must manually restore any nondefault CMOS settings being used by the system.

21. B. The BIOS stores the PnP information it collects from the devices in a special section of the CMOS RAM known as the *Extended System Configuration Data (ESCD)* area. This information is stored in the same manner as standard BIOS settings are stored. The BIOS and the operating system both access the ESCD area each time the system is restarted to see if any information has changed. This enables the BIOS and the operating system to work together in sorting out the needs of the installed devices and assigning them needed system resources.

22. C. The Standard CMOS setup screens from various BIOS manufacturers all provide the same basic information. For example, they can be used to set the date and time via the system clock/calendar. During the startup process, the operating system acquires the time and date information from the CMOS RTC module. This information is updated in the system once every second.

23. A. The ECP mode supports high-throughput DMA operations for both forward- and reverse-direction transfers.

24. A. The ECP mode offers higher performance than either the SPP or the EPP mode.

25. A. Because both of the advanced parallel port modes operate in a bidirectional, half-duplex manner, they require an IEEE-1284-compliant cable. Standard parallel cables designed for older SPP operations may not support these qualities.

26. B. The Drive A: option in the Drive Seek Sequence setting should be enabled if the system cannot boot to the hard-disk drive and you have a clean boot disk or emergency repair floppy. If you disable the A: seek function in the CMOS setup utility (by not selecting it as part of the boot seek sequence), you will not be able to use the A: drive to troubleshoot hard-drive problems. The system then would never access the floppy drive to see if it had a bootable disk in it; however, you can always enter the CMOS setup utility and include it as part of the troubleshooting process.

27. D. The Supervisory password is used to control access to the system's CMOS setup utility. Because this system is opened for public use, setting a User password would prevent users from accessing the system. The Supervisory password will prevent intentional malicious access to the CMOS where users could disable the system.

28. A. The User password option enables you to establish password access to the systems that you can share with your employees. This will prevent other employees from accessing the systems without giving your employees access to the CMOS setup utility.

29. A. The first line of system protection in this situation is setting a Supervisory password in the CMOS Setup utility to prevent users from accessing and manipulating the system's configuration settings.

Challenge Solutions

1. You can potentially upgrade your Pentium II/Slot 1 machines to Pentium III class microprocessors that will run at up to 1GHz.

2. The three-bank split bank slot arrangement has separated the memory into a 128MB section for the first slot and only 128MB for the second bank of two slots. These devices are not compatible with the organization of the board's slot configuration. You need to obtain the system board's user's manual to determine what types and sizes of memory devices can be used. (If this occurs when you are using the specified types of memory devices, you may have a bad DIMM device in one of the slots.)

3. You must go into the CMOS Setup utility and make sure that the CD-ROM drive is one of the options selected in the Drive Seek Sequence.

4. There are several things that you should do to make this modem work in your system. The item we are most interested in, at this point, is the configuration information required by the CMOS. Older BIOS versions required that you manually disable the COM2 setting and reserve an IRQ setting for the modem in the PnP/PCI Configuration window. Windows 2000 and Windows XP operating systems will detect the presence of an ISA device and reserve a set of resources for it; however, you are still required to supply an acceptable device driver program for the device.

5. If you consider the nature of the two devices, you will realize that the scanner is basically an input device (actually a bidirectional device), so its data must move back to the parallel port, whereas the printer is an output device, so information normally travels from the port to the printer. Check the parallel cables to make sure that they are IEEE-1284 compliant. The port must be configured for bidirectional support in the CMOS. Check the CMOS settings to make sure that EPP or ECP modes are selected.